Xilinx 7 series PCB point list

『 ———————————— Configuration ———————————— 』

首先是Configuration時所需要作設定的硬體週邊的電路,假若這個地方有問題,那肯定要重新layout,

以下是 SPI Mode 的設定的參考電路圖

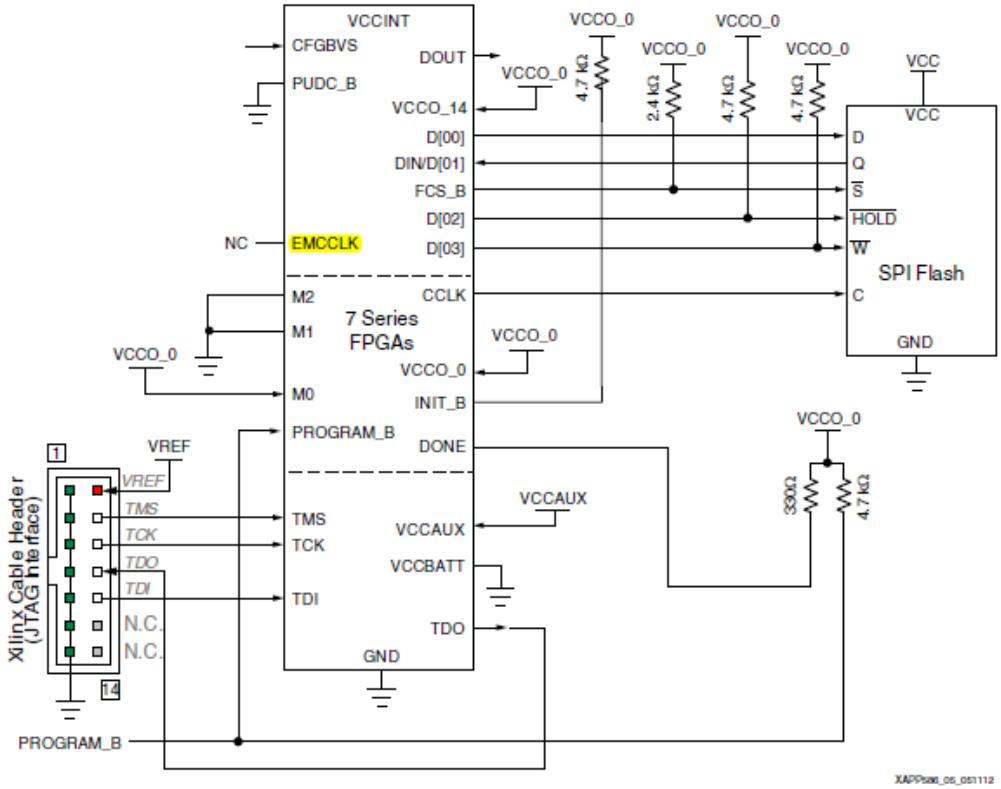


Figure 5: **7 Series FPGA SPI Flash x4 Configuration Schematic**

http://www.xilinx.com/support/documentation/user_guides/ug470_7Series_Config.pdf

Xilinx® 7 series devices have five configuration interfaces. Each configuration interface corresponds to one or more configuration modes and bus width, shown in Table 2-1. For detailed interface timing information, see the respective 7 series FPGAs data sheet.

Table 2-1: **7 Series FPGA Configuration Modes**

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	x1	Output
Master SPI	001	x1, x2, x4	Output
Master BPI	010	x8, x16	Output
Master SelectMAP	100	x8, x16	Output
JTAG	101	x1	Not Applicable
Slave SelectMAP	110	x8, x16, x32(1)	Input
Slave Serial(2)	111	x1	Input

Notes:

1. The Slave SelectMAP x16 and x32 bus widths do not support AES-encrypted bitstreams.
2. This is the default setting due to internal pull-up resistors on the Mode pins.

M0/M1/M2

這 3pin 主要的功能是選擇 FPGA Load Code 的方式,總共有以下幾種模式,所以我們建議最好是分別都作 pull up/down (公板線路上是 200 ~ 1K)

PS:這幾 PIN 並不是 multi-function,所以不能當一般 IO 使用!!!!!!

7series FPGA CCLK 是不能當作 User I/O PIN,所以如果需要作 Remote Update Flash 應用的話,需要另外找一個 PIN 並接來當作更新 Flash 的 Clock

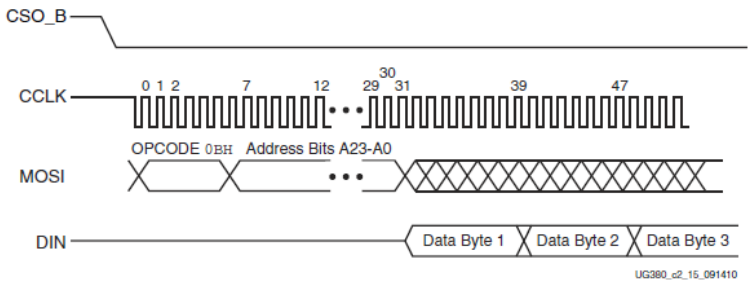


Figure 2-11: **7 Series FPGA SPI x1 Mode Sequence**

INIT_B / DONE /PROGRAM_B

這 3pin 也是變成非 dual function pin,不同於其他 Xilinx family device 可以拿來當作一般的 IO 使用

INIT_B << 主要的功能在告知 FPGA 硬體及電源已經 ready 可以讀取 Flash 資料了,這 Pin 需要在 power on 時維持在 high, 所以 pull up 是保險的作法,雖然 FPGA 內部會 pull up 但很 weak.

DONE << 這 PIN 是顯示 FPGA 是否正常動作的專屬 IO,一般我們會接一個 LED 來作為判斷 FPGA 是否正常運作的依據, 但這一 Pin 需要在 power on 時維持在 high,直到 FPGA Configuration 結束時

< done pin 的動作是 Low → Hz → High >

PROGRAM_B << 一般會接到 high,它的功用是 Low to High 時 FPGA 會重新 reload flash 資料,重新配置 FPGA

PUDC_B << 這 PIN 的功能是決定 FPGA 在 configuration 時,IO 的狀態,建議是分別 pull /down,如果完全不在意 configuration IO 的 default 狀能是可以不管它的.

這可以參考下表

PUDC_B	14	Multi-function	Input	Pull-Up During Configuration (bar) Active-Low PUDC_B input enables internal pull-up resistors on the SelectIO pins after power-up and during configuration. • When PUDC_B is Low, internal pull-up resistors are enabled on each SelectIO pin. • When PUDC_B is High, internal pull-up resistors are disabled on each SelectIO pin. PUDC_B must be tied either directly, or via a 1 kΩ (or stronger) resistor, to V_{CCO_14} or GND. ***Caution!*** Do not allow this pin to float before and during configuration.

CFGBVS 是用來設定 BANK0 的電壓用,為什麼會需要的原因是大部份的 Config 跟 XADC PIN 都在 BANK0 由其是 CCLK……因為 MOSI/DIN/FCS_B….可能該 BANK 會因為設計而使用不同的電壓,造成一些困擾..

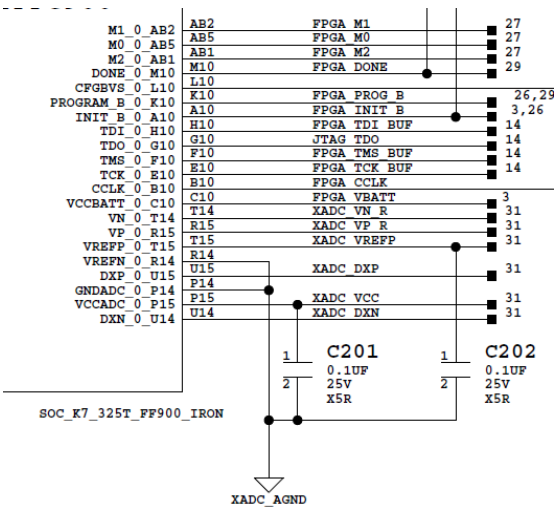
Table 2-5: **CFGBVS Pin Connection for Bank V_{CCO} Supplies and I/O Signal Voltages**

CFGBVS Pin Connection	Supported Bank 0 V_{CCO_0} Supply and I/O Signal Voltages
V_{CCO_0} (3.3V or 2.5V)	3.3V or 2.5V
GND	1.8V maximum

http://www.xilinx.com/support/documentation/data_sheets/ds182_Kintex_7_Data_Sheet.pdf

【AES/ eFUSE.】Xilinx 有提供 bitstream security 的功能,如果需要的話可以選擇 Key 是燒斷或是外掛電池的方式

http://csrc.nist.gov/publications/fips/fips197/fips-197.pdf



V_{CCBRAM}	Supply voltage for the block RAM memories	–0.5	1.1	V

V_{CCBATT}	Key memory battery backup supply	–0.5	2.0	V

依照 Xilinx DC Datasheet 所示,如果 Config 是使用 Master Mode 在讀取 Flash 時,在 Xilinx 軟體 CCLK 最快可以設為 66Mhz, 但是它的速度正負落差可能會有 50%...

http://www.xilinx.com/support/documentation/boards_and_kits/kc705_Schematic_xtp132_rev1_1.pdf Xilinx Kit-KC705

$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK	±50	±50	±50	±50	%, Max

如果嫌 CCLK 只能有 66Mhz,不夠快的話,那可以用外部給的 Clock,最快可以支持 100Mhz,但要給專屬的 IO PIN

F_{EMCCK}	External master CCLK frequency	100.00	100.00	100.00	70.00	MHz, Max

Xilinx ISE Configuration options

Property Name	Value
Configuration Rate	3
Configuration Clk (Configuration Pins)	3 6 9 12 16 22 26 33 40 50 66
Configuration Pin M0	
Configuration Pin M1	
Configuration Pin M2	
Configuration Pin Program	
Configuration Pin Done	
Configuration Pin Init	
JTAG Pin TCK	

Design Considerations for the External Master Clock

When using the external master clock (EMCCLK) as a configuration clock source, EMCCLK must be included in the user's design. Not doing so results in the FPGA failing to complete the start-up sequence. No special design requirements are needed when using the internal oscillator for FPGA configuration.

Xilinx 7 Series 並沒有一份專門的文件告知 Pinout Name,但可以透過 ug475 上的連結下載(FAE 可以提供 OrcAD)

http://www.xilinx.com/support/documentation/user_guides/ug475_7Series_Pkg_Pinout.pdf

http://www.xilinx.com/support/packagefiles/kintex-7-pkgs.htm

Table 2-2: **Kintex-7 FPGAs Package/Device Pinout Files**

Device	FB484/ FBG484	FB676/ FBG676	FB900/ FBG900	FF676/ FFG676	FF900/ FFG900	FF901/ FFG901	FF1156/ FFG1156
XC7K70T	FBG484	FBG676					
XC7K160T	FB484/ FBG484	FB676/ FBG676		FF676/ FFG676			
XC7K325T		FB676/ FBG676	FB900/ FBG900	FF676/ FFG676	FF900/ FFG900		
XC7K355T						FF901/ FFG901	
XC7K410T		FB676/ FBG676	FB900/ FBG900	FF676/ FFG676	FF900/ FFG900		
XC7K420T						FF901/ FFG901	FF1156/ FFG1156
XC7K480T						FF901/ FFG901	FF1156/ FFG1156

下表是有關 Aritex7 / Kintex7 Configuration 需要的 SPI Flash Memory Size

http://www.xilinx.com/support/documentation/user_guides/ug470_7Series_Config.pdf

Table 1-1: **Bitstream Length**

Device	Configuration Bitstream Length (bits)	Minimum Configuration Flash Memory Size (Mb)	JTAG/Device IDCODE[31:0] (hex)(1)	JTAG Instruction Length (bits)	Super Logic Regions
Artix-7 Family					
7A100T	30,606,304	32	X3631093	6	N/A
7A200T	77,845,216	128	X3636093	6	N/A
Kintex-7 Family					
7K70T	24,090,592	32	X3647093	6	N/A
7K160T	53,540,576	64	X364C093	6	N/A
7K325T	91,548,896	128	X3651093	6	N/A
7K355T	112,414,688	128	X3747093	6	N/A
7K410T	127,023,328	128	X3656093	6	N/A
7K420T	149,880,032	256	X3752093	6	N/A
7K480T	149,880,032	256	X3751093	6	N/A

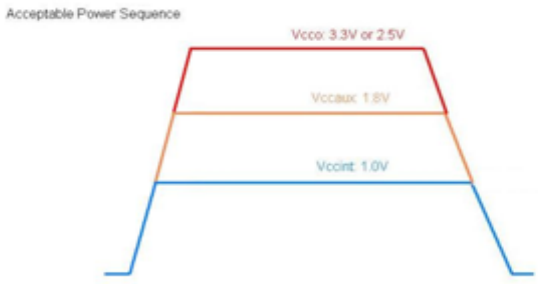
『 Power sequence 』

Xilinx 7 series 是有 power sequence 主要是針對 3.3V

原則上是先關後關

VCCINT >> VCCAUX >> VCCO --- Power On

VCCO >> VCCAUX >> VCCINT -- Power Off



VCCAUX to VCCO(HR) Requirement – Data Sheet

7 Series Devices with High Range (HR) I/O banks with a VCCO of 2.5V or 3.3V must meet the following requirements:

Power-up

VCCAUX must be raised before VCCO(HR at 2.5V-3.3V)

Power-down

VCCO(HR at 2.5V-3.3V) must be lowered before VCCAUX

原則上 power sequence 是比較針對有 3.3V 的需求的使用者,Xilinx 7 series 有 HP/HR Bank 的區分

【HP】是有高效能的 IO,但是最高只能支持 1.8V 的 IO Type （ 若拿來作 DDR/LVDS 都會比 HR 的速度來的快許多)

【HR】的是可以支持 1.2~3.3V 的 IO Type,好處是彈性很大,但效能稍差了點,僅管如此 ddr3 也是能到 800Mhz,LVDS 可以 1.25G

一般 7 系列的 device,一個 BANK 是 50 支 IO

HP Bank 是可以支持 LVDS Standard Xilinx 有 Answers

http://www.xilinx.com/support/answers/41408.htm

7 series 如何只使用一個 BANK 來支持 16 bit DDR component

http://www.xilinx.com/support/answers/41752.htm

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

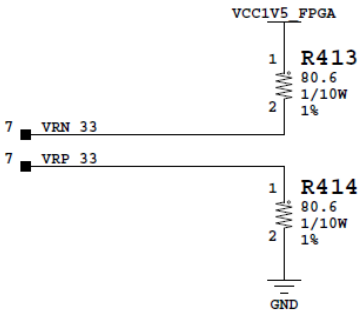
- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

『 ——————————DDR3 —————————— 』

DDR的IO原則上都是透過Xilinx MIG(Memory Interface Generator)產生的,所以只要確認與(.UCF)中的內容與DDR component或DIMM對接就好,並不會有太大的問題,MIG也可以依照硬體Layout需求作一些PINOUT調整,但調整過的PINOUT一定要再經過MIG作DRC Check!!!

其中比較困擾的地方是HP/HR Bank不同共用在一個DDR Controller上,所以在像7K70T的device上,會發生只有兩個HP BANK卻無法接DIMM的麻煩.....

Xilinx 在7series中可以設定DDR Memory ODT/TCI的功能是否開?,一般都會使用預設值開啟的.
如果把MIG選用HR,在DCI的選項中確實是沒有效用的,但是MIG會自動加入IN_TERM = UNTUNED_SPLIT_50,這與DCI的功能是相同的,所以不需要在PCB上加電阻,若是MIG在HP BANK那只要有使用到的BANK,兩PIN硬體都要接.



- VRN and VRP are used for the digitally controlled impedance (DCI) reference for banks that support DCI. DCI cascade is permitted; however, only the RESET_N can be placed on the spare VRN/VRP pins.

上面的設定主要是跟熱與功耗有關如果 termination 設定在 FPGA 內部,則會有熱的問題要處理,
反之如果留在電路板上,則會有空間的考量,這部份需視使用者當時的情況來作決定
Xilinx的ddr3 controller會需要一組200Mz的Clock,在公板上是使用differential
因為FPGA內有倍頻的原件像MMCM/PLL等等,所以只要提供一組基頻最好是200的公因素,像是50,100之類的,就可以透過內部原件產生這個頻率, differential或是Single-End並沒有限制.

Xilinx 針對 DDR layout 有提供相關的參考文件
http://www.xilinx.com/support/documentation/white_papers/wp420-DDR3-SI-PCB.pdf
http://www.xilinx.com/support/documentation/ip_documentation/ug586_7Series_MIS.pdf

有關 Die to Pad 的距離問題是否要考量??
如果 DDR3 是工作在 1066Mhz 以上的 data-rate,那 Xilinx 是建議可以作 IBIS 模擬,上述的問題也是需要被考慮的
Xilinx 有工具可以產生這份文件副檔名是.pkg

『 7series 會用到的電源表 』

Table 2: **Recommended Operating Conditions** (1)

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT} (2)	Internal supply voltage	0.97	1.00	1.03	V
	For -2L (0.9V) devices: internal supply voltage	0.87	0.90	0.93	V
V_{CCBRAM} (2)	Block RAM supply voltage	0.97	1.00	1.03	V
	For -2L (0.9V) devices: block RAM supply voltage	0.87	0.90	1.03	V
V_{CCAUX}	Auxiliary supply voltage	1.71	1.80	1.89	V
V_{CCO} (3)(4)	Supply voltage for 3.3V HR I/O banks	1.14	–	3.465	V
	Supply voltage for 1.8V HP I/O banks	1.14	–	1.89	V
V_{CCAUX_IO}	Auxiliary supply voltage when set to 1.8V	1.71	1.80	1.89	V
	Auxiliary supply voltage when set to 2.0V	1.94	2.00	2.06	V
V_{IN} (5)	I/O input voltage	–0.20	–	V_{CCO} + 0.2	V
	I/O input voltage for V_{REF} and differential I/O standards	–0.20	–	2.625	V
I_{IN} (6)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
V_{CCBATT} (7)	Battery voltage	1.0	–	1.89	V
GTX Transceiver					
$V_{MGTAVCC}$ (8)	Analog supply voltage for the GTX transceiver QPLL frequency range ≤ 10.3125 GHz (9)(10)	0.97	1.0	1.08	V
	Analog supply voltage for the GTX transceiver QPLL frequency range > 10.3125 GHz	1.02	1.05	1.08	V
$V_{MGTAVTT}$ (8)	Analog supply voltage for the GTX transmitter and receiver termination circuits	1.17	1.2	1.23	V
$V_{MGTVCCAUX}$ (8)	Auxiliary analog QPLL voltage supply for the transceivers	1.75	1.80	1.85	V
Symbol	**Description**	**Min**	**Typ**	**Max**	**Units**
$V_{MGTAVTTRCAL}$ (8)	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	1.17	1.2	1.23	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C

Notes:

1. All voltages are relative to ground.
2. V_{CCINT} and V_{CCBRAM} should be connected to the same supply.
3. Configuration data is retained even if V_{CCO} drops to 0V.
4. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
5. The lower absolute voltage specification always applies.
6. A total of 200 mA per bank should not be exceeded.
7. V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX}.
8. Each voltage listed requires the filter circuit described in UG476: *7 Series FPGAs GTX/GTH Transceiver User Guide*.
9. For data rates ≤ 10.3125 Gb/s, $V_{MGTAVCC}$ should be 1.0V ±3% for lower power consumption.
10. For lower power consumption, $V_{MGTAVCC}$ should be 1.0V ±3% over the entire CPLL frequency range.

http://www.xilinx.com/support/documentation/data_sheets/ds182_Kintex_7_Data_Sheet.pdf **Kintex7 datasheet**

MGTAVCC / MGTAVTT / MGTAVCCAUX / MGTAVTTRCAL << 這些腳PIN,儘管都沒有用到任何一組GTP,還是建議要給電源 http://www.xilinx.com/support/documentation/boards_and_kits/kc705_Schematic_xtp132_rev1_1.pdf **KC705**

或是參考Xilinx Transceivers user guide

http://www.xilinx.com/support/documentation/user_guides/ug482_7Series_GTP_Transceivers.pdf

Unused GTP Quad Power Supply Group

If none of the GTP Quads in a power supply group are used in the application, the GTP Quad device pins can be connected as shown in Table 5-3.

Table 5-3: **Unused GTP Quad Column Connections**

Pin or Pin Pair of the Unused GTP Quad	Connection
MGTAVCC	GND
MGTAVTT	GND
MGTREFCLKP/MGTREFCLKN	Float
MGTRXP/MGTRXN	GND
MGTTXP/MGTTXN	Float
MGTRREF(1)	GND

Notes:

1. This is the only scenario when the MGTRREF pins can be connected to ground. In all other scenarios, these pins must be connected for normal operation.

Partially Unused GTP Quad Power Supply Group

If only a portion of the GTP Quads in a power supply group is used, the pins for unused GTP Quads must be connected as shown in Table 5-4. Notice for this case, the power supply pins must be connected to the appropriate power supply operating voltage and the MGTRREF pin is connected to MGTAVTT through a 100Ω resistor.

Table 5-4: **Unused GTP Quad Column Connections**

Pin or Pin Pair of the Unused GTP Quad	Connection
MGTAVCC	AVCC
MGTAVTT	AVTT
MGTREFCLKP/MGTREFCLKN	Float
MGTRXP/MGTRXN	GND
MGTTXP/MGTTXN	Float
MGTRREF	MGTAVTT through a 100Ω resistor

ZYNQ 若沒有用到 ADC function 則以下 ADC pin 要如何處理?
DXN, DXP, VREFP, VREFN, VP, VN, VCCADC, GNDADC
VCCADC, GNDADC 兩 PIN 要接,VREFP, VREFN, VP, VN 可以選擇接地,VP, VN,至於這兩 PIN 其實是還好,沒特別規定
http://www.xilinx.com/support/documentation/user_guides/ug480_7Series_XADC.pdf

Table 1-1: **XADC Package Pins**

Package Pin	Type	Description
V_{CCADC_0}	Power supply	This is the analog supply pin for the ADCs and other analog circuits in the XADC. It can be tied to the 1.8V V_{CCAUX} supply however in a mixed-signal system the supply should be connected to a separate 1.8V analog if available. See Analog Power Supply and Ground (V_{CCADC} and GNDADC), page 69 for more information. This pin should never be tied to GND. The pin should be tied to V_{CCAUX} even if the XADC is not being used.
GNDADC_0	Power supply	This is the ground reference pin for the ADCs and other analog circuits in the XADC. It can be tied to the system ground via an isolating ferrite bead as shown in Figure 1-2. In a mixed-signal system this pin should be tied to an analog ground plane if available, in which case the ferrite bean is not required. See Analog Power Supply and Ground (V_{CCADC} and GNDADC), page 69 for more information. This pin should always be tied to GND even if the XADC is not being used.

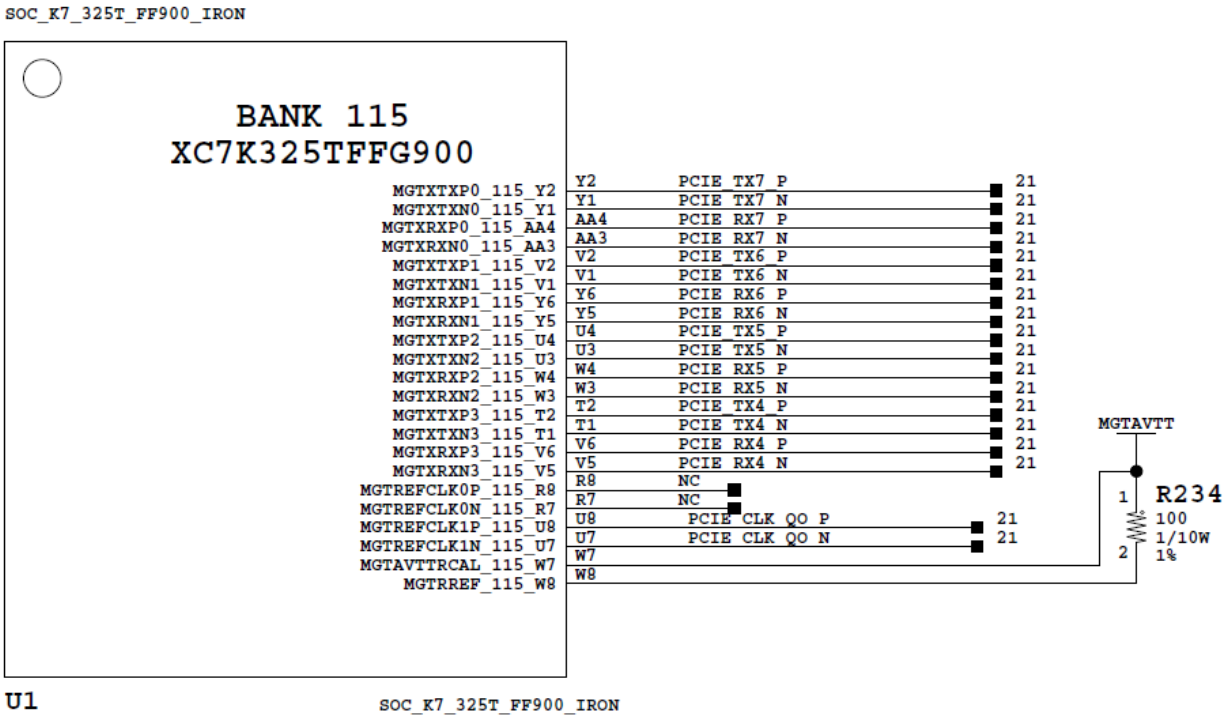
V_{REFP_0}	Reference voltage input	This pin should be tied to an external 1.25V accurate reference IC (±0.2%) for best performance of the ADCs. It should be treated as an analog signal that together with the V_{REFN} signal provides a differential 1.25V voltage. By connecting this pin to GNDADC (see Figure 1-2) an on-chip reference source (±1%) is activated. This pin should always be connected to GNDADC if an external reference is not supplied. See Reference Inputs (V_{REFP} and V_{REFN}), page 69 for more information.
V_{REFN_0}	Reference voltage input	This pin should be tied to GND pin of an external 1.25V accurate reference IC (±0.2%) for best performance of the ADCs. It should be treated as an analog signal that together with the V_{REFP} signal provides a differential 1.25V voltage. This pin should always be connected to GND even if an external reference is not supplied. See Reference Inputs (V_{REFP} and V_{REFN}), page 69 for more information.
V_{P_0}	Dedicated analog input	This is the positive input terminal of the dedicated differential analog input channel (V_P/V_N). The analog input channels are very flexible and support multiple analog input signal types. For more information see Analog Inputs, page 26. This pin should be connected to GND if not used.
V_{N_0}	Dedicated analog input	This is the negative input terminal of the dedicated differential analog input channel (V_P/V_N). The analog input channels are very flexible and support multiple analog input signal types. For more information see Analog Inputs, page 26. This pin should be connected to GND if not used.

『 PCIe / Transceivers 』

PCIe 的 IO 原則上都是透過 Xilinx CoreGen 產生的,所以只要依照.ucf 就能找到對應的 MGT 位置

Xilinx IP 在設定上的 System 可輸入 100Mhz/250Mhz 兩種

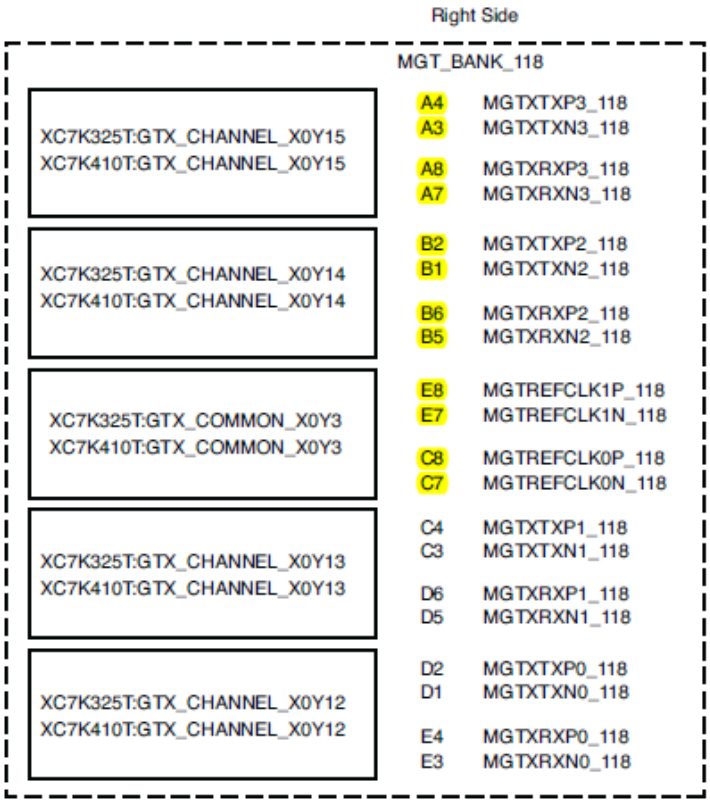
一般都會使用主機板提供的 100Mhz



http://www.xilinx.com/support/documentation/ip_documentation/ug477_7Series_IntBlock_PCIe.pdf

Xilinx PCIe IP 產生時會使用 Transceivers 對應的位置作表示,如:X0Y15/X0Y13..之類的

但可以在 ug477 中找到真實的 IOB Pad.



http://www.xilinx.com/support/documentation/user_guides/ug476_7Series_Transceivers.pdf

Xilinx 有 Tandem 作 partial reconfiguration PCIe core 的功能,能夠符合 PC 100ms reset 的要求

『 ———————————— Other Point ———————————— 』

SSO(simultaneous switching noise)使用上的限制,可以將 PIN Define(.UCF)檔案輸入給 Xilinx PlanAhead 的工具就能作預估

【Xilinx 支持的 SPI Flash 清單...】

Table 2-11: **Supported SPI Flash Devices**

Device
Micron N25Q 3.3V
Micron N25Q 1.8V
Micron M25P
Winbond W25Q
Spansion S25FL

FBG676 和 FFG676 是 pin to pin 相容,但是硬體 VCC-GND 的電容數量大小要參照 FFG

Required PCB Capacitor Quantities

Table 2-1 lists the PCB decoupling capacitor guidelines per V_{CC} supply rail for Kintex-7 devices.

Table 2-1: **Required PCB Capacitor Quantities per Device: Kintex-7 Devices(1)**

Package	Device	V_{CCINT}				V_{CCBRAM}				V_{CCAUX}			V_{CCAUX_IO}			V_{CCO} per Bank	
		Req'd µF	330 µF	100 µF	4.7 µF	Req'd µF	330 µF	100 µF	4.7 µF	Req'd µF	47 µF	4.7 µF	Req'd µF	47 µF	4.7 µF	Req'd µF	100 µF
FBG484	XC7K70T	265	1			61		1	2	65	1	2	35	1	2	100	1
FBG484	XC7K160T	540	2			101		1	3	65	1	2	35	1	2	100	1
FBG676	XC7K70T	265	1			61		1	2	70	1	2	35	1	2	100	1
FBG676	XC7K160T	540	2			101		1	3	88	2	2	53	1	3	100	1
FBG676	XC7K325T	1106	3		5	200		2	5	88	2	2	53	1	3	100	1
FBG676	XC7K410T	1645	5		10	358	1		9	88	2	2	53	1	3	100	1
FBG900	XC7K325T	1106	3		5	200		2	5	123	3	3	53	1	3	100	1
FBG900	XC7K410T	1645	5		10	358	1		9	123	3	3	53	1	3	100	1
FFG676	XC7K160T	540	2			101		1	3	88	2		53	1		100	1
FFG676	XC7K325T	1106	3			200		2	5	88	2		53	1		100	1
FFG676	XC7K410T	1645	5			358	1		9	88	2		53	1		100	1
FFG900	XC7K325T	1106	3			200		2	5	123	3		53	1		100	1
FFG900	XC7K410T	1645	5			358	1		9	123	3		53	1		100	1

Notes:
1. PCB Capacitor specifications are listed in Table 2-2.
2. Total includes all capacitors for all supplies, except for the MGT supplies MGTAVCC, MGTVCCAUX, and MGTAVTT, which are covered in UG476, *7 Series FPGAs GTX Transceivers User Guide*. The values in this table account for the number of I/O banks in the device.

Power Estimator 工具: http://www.xilinx.com/products/design_tools/logic_design/xpe.htm

Subject: RE: <CASE:937738> KC705 - characteristic impedance about the DDR3 PCB layout

Hi Leo，

I've confirmed the layout. The impedance is 40 ohm.

Best regards,

XiBin

ANSTek Xilinx FAE Leo>Lee