Xilinx PLD General Application

Answer Technology Co., Ltd.
Application Dept.
FAE Leo Lee

XILINX
ANStek

Xilinx CPLD Products Table

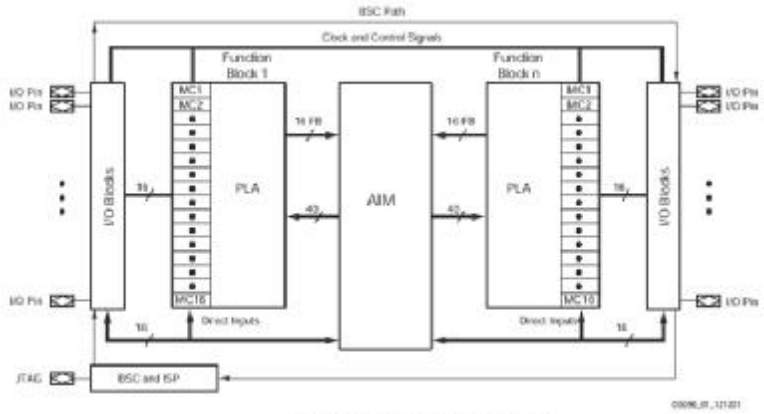
Table 3: **CoolRunner-II CPLD Family Packages and I/O Count**

	XC2C32A	XC2C64A	XC2C128	XC2C256	XC2C384	XC2C512
QFG32(1)	21	-	-	-	-	-
VQ44	33	33	-	-	-	-
VQG44(1)	33	33	-	-	-	-
QFG48(1)	-	37	-	-	-	-
CP56	33	45	-	-	-	-
CPG56(1)	33	45	-	-	-	-
VQ100	-	64	80	80	-	-
VQG100(1)	-	64	80	80	-	-
CP132	-	-	100	106	-	-
CPG132(1)	-	-	100	106	-	-
TQ144	-	-	100	118	118	-
TQG144(1)	-	-	100	118	118	-
PQ208	-	-	-	173	173	173
PQG208(1)	-	-	-	173	173	173
FT256	-	-	-	184	212	212
FTG256(1)	-	-	-	184	212	212
FG324	-	-	-	-	240	270
FGG324(1)	-	-	-	-	240	270

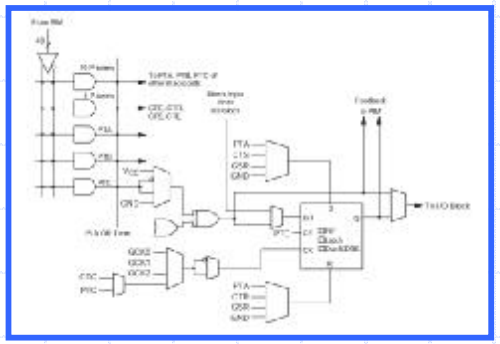
Notes:
1. The letter "G" as the third character indicates a Pb-free package.

CPLD【Complex Programmable Logic Device】

CoolRunner-II



CoolRunner-II CPLD Architecture



XC9500XL

	XC9536	XC9572	XC95108	XC95144	XC95216	XC95288
44-Pin VQFP	34	-	-	-	-	-
44-Pin PLCC	34	34	-	-	-	-
48-Pin CSP	34	-	-	-	-	-
84-Pin PLCC	-	69	69	-	-	-
100-Pin TQFP	-	72	81	81	-	-
100-Pin PQFP	-	72	81	81	-	-
160-Pin PQFP	-	-	108	133	133	-
208-Pin HQFP	-	-	-	-	166	168
352-Pin BGA	-	-	-	-	166	192

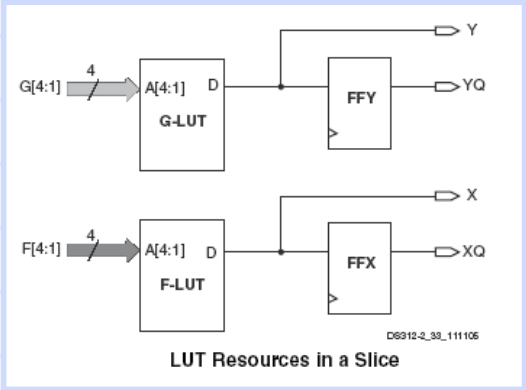
1. Most packages available in Pb-Free option. See individual data sheets for more details.

Xilinx XC3S50/200AN Products Table

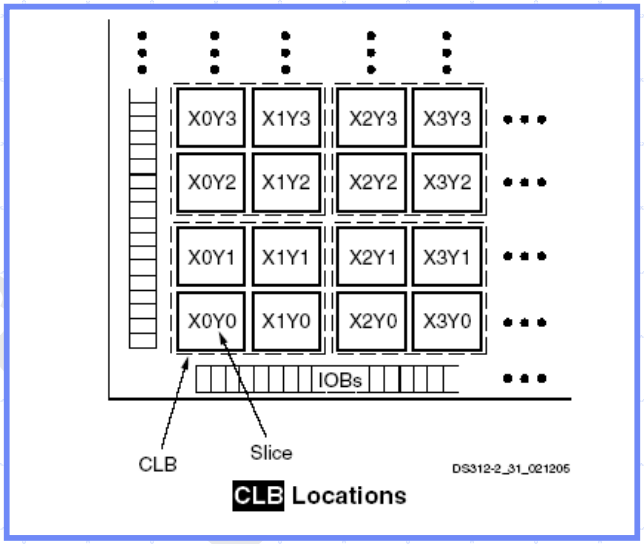
Logic Cell (LUT) x 0.7 ~= CPLD Microcell

Extended Spartan-3A Family
Optimized for Lowest Total Cost

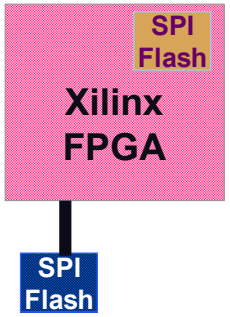
	Part Number	XC3S50A/AN	XC3S200A/AN
Logic Resources	System Gates[1]	50K	200K
	Slices[2]	704	1,792
	Logic Cells	1,584	4,032
	CLB Flip-Flops	1,408	3,584
Memory Resources	Maximum Distributed RAM (Kb)	11	28
	Block RAM (18 Kb each)	3	16
	Total Block RAM (Kb)	54	288
Non-Volatile Capability	Single Chip Option	Yes	Yes
	User Flash (Kb)[3]	- / 627	- / 3,054
Clock Resources	Digital Clock Managers (DCMs)	2	4
I/O Resources	Maximum Single-Ended I/Os	144 / 108	248 / 195
	Maximum Differential I/O Pairs	64 / 50	112 / 90
	I/O Standards Supported	LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, SSTL3 Class I, SSTL3 Class II, SSTL2 Class I, SSTL2 Class	
Embedded Hard IP Resources	Multipliers/DSP48A Blocks	3	16
	Device DNA Security	Yes	Yes
Speed Grades	Commercial	-4, -5	-4, -5
	Industrial	-4	-4
Configuration	Configuration Memory (Mb)	0.4	1.2
Package[4]	Footprint Size		
VQFP Packages (VQ): Very thin QFP (0.5 mm lead spacing)			
VQ100	16 x 16 mm	68 / -[7]	68 / -[7]
TQFP Packages (TQ): Thin QFP (0.5 mm lead spacing)			
TQ144	22 x 22 mm	108 / 108	
BGA Packages (FT): Wire-bond, fine-pitch, thin BGA (1.0 mm ball spacing)			
FT256	17 x 17 mm	144 / -[7]	195 / 195
Chip Scale Packages (CS): Wire-bond, chip-scale, BGA (0.8 mm ball spacing)			
CS484	19 x 19 mm		
BGA Packages (FG): Wire-bond, fine-pitch, BGA (1.0 mm ball spacing)			
FG320	19 x 19 mm		248 / -[7]
FG400	21 x 21 mm		



LUT Resources in a Slice



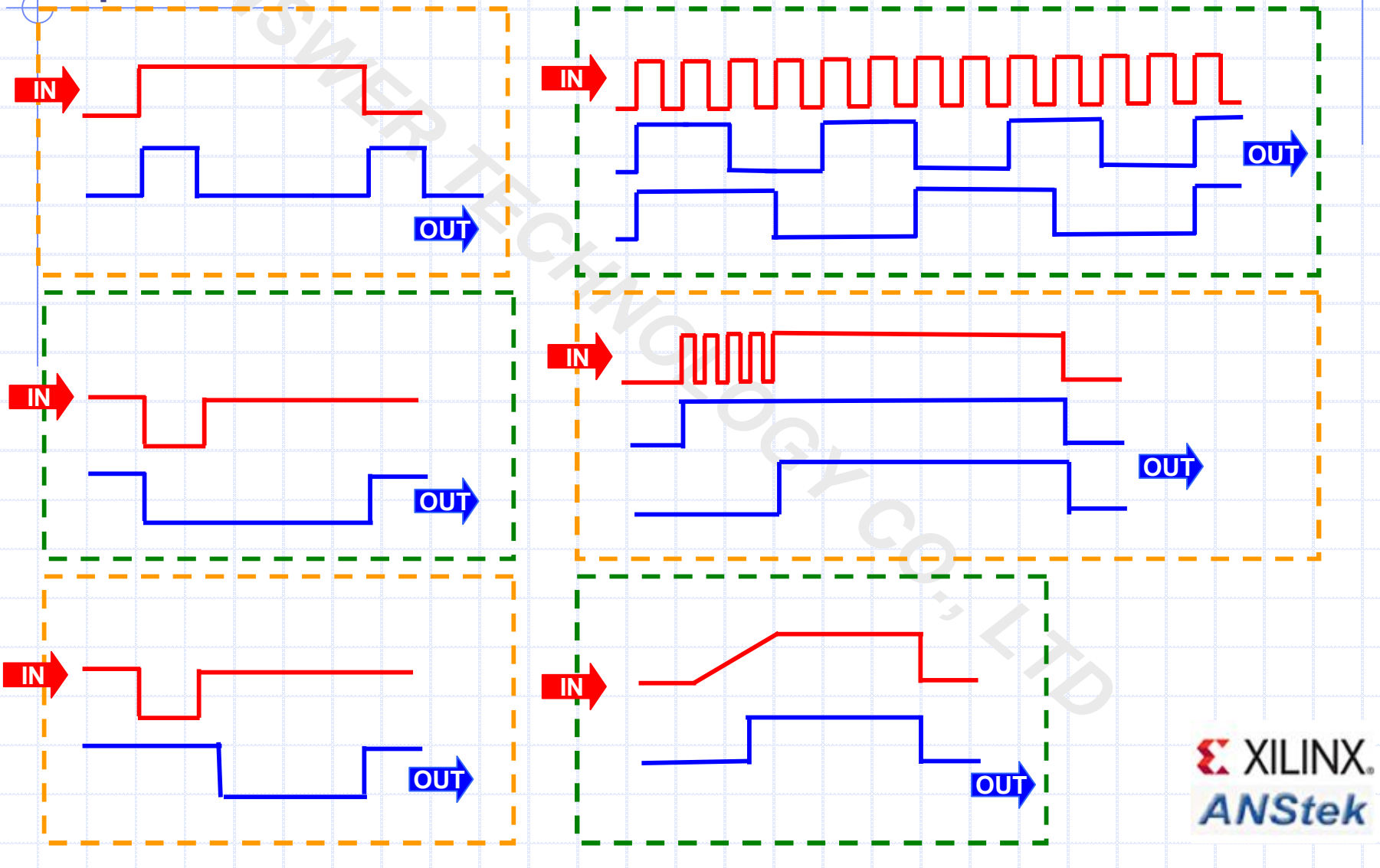
CLB Locations



XILINX
ANStek

PLD Timming Simple Application

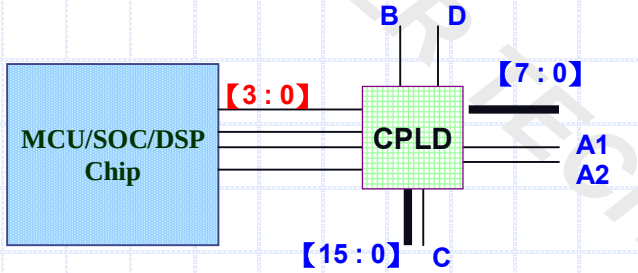
Example



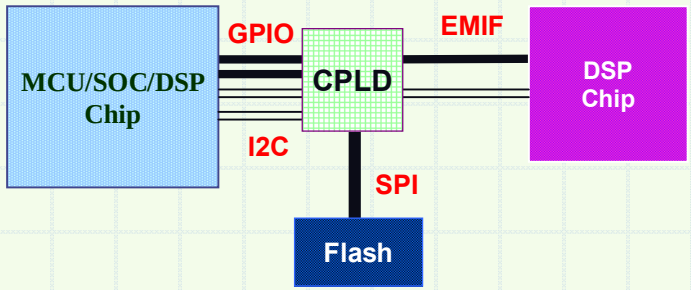
XILINX
ANStek

PLD IO Function Application

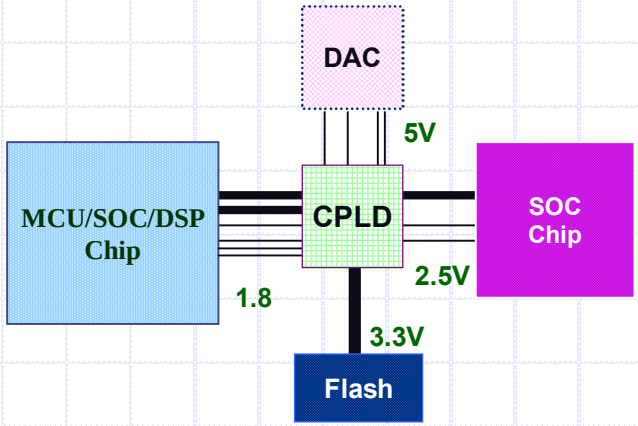
I/O Expansion



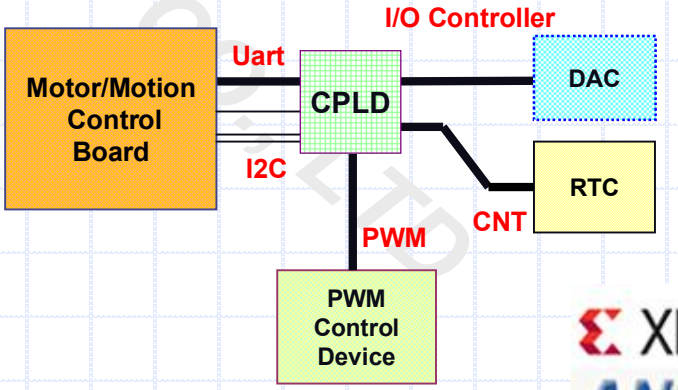
Interface Bridge / Transforms



Level Shift



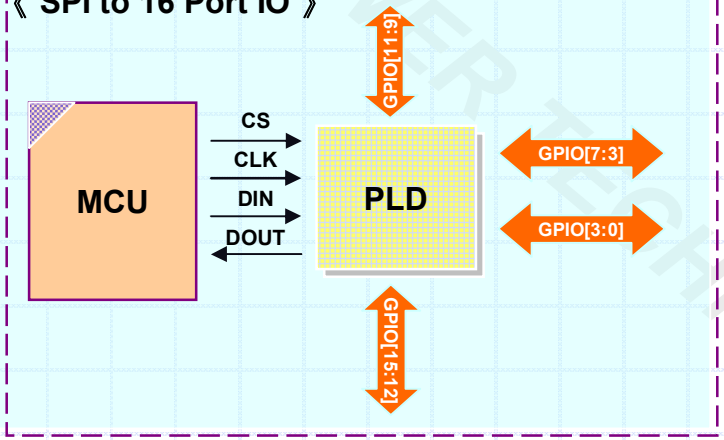
IO Controller/ PWM



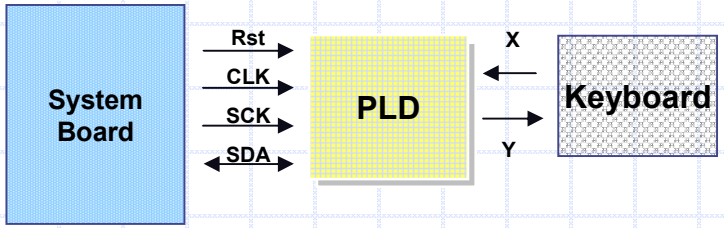
XILINX
ANStek

Anstek PLD Reference design - 1

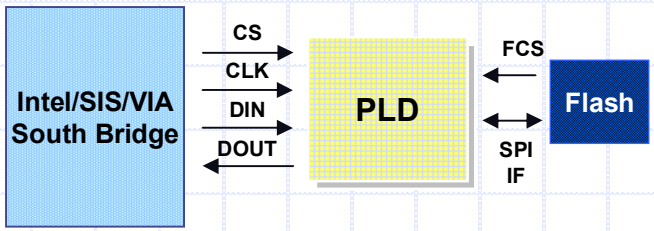
《 SPI to 16 Port IO 》



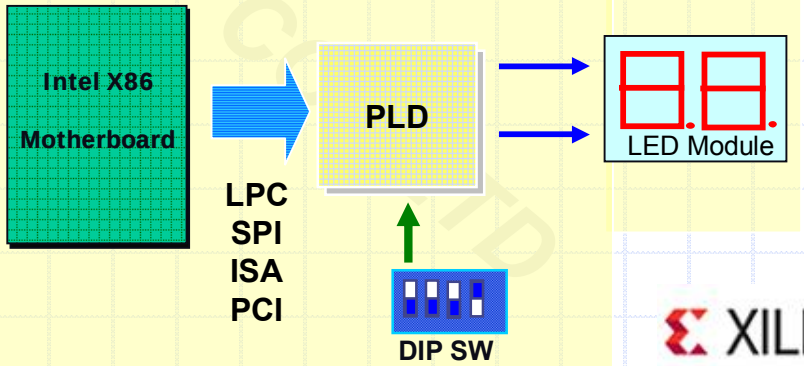
《 KeyScan and data decoder 》



《 SPI Flash Data Read Only 》



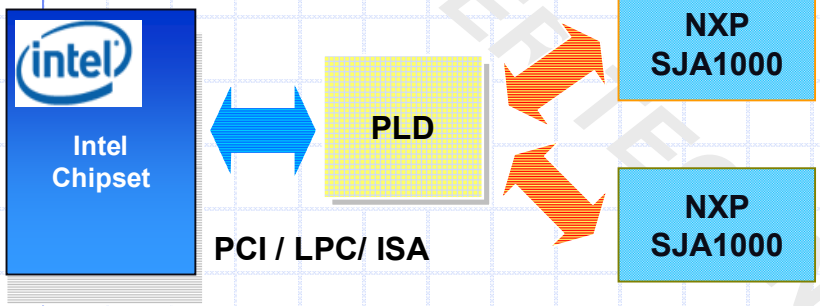
《 Motherboard 80 Port Debug Card 》



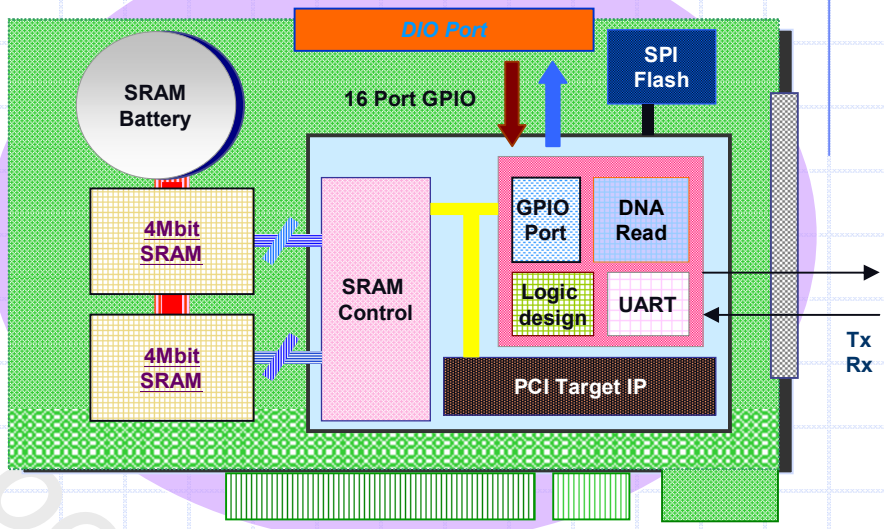
XILINX
ANStek

Anstek PLD Reference design - 2

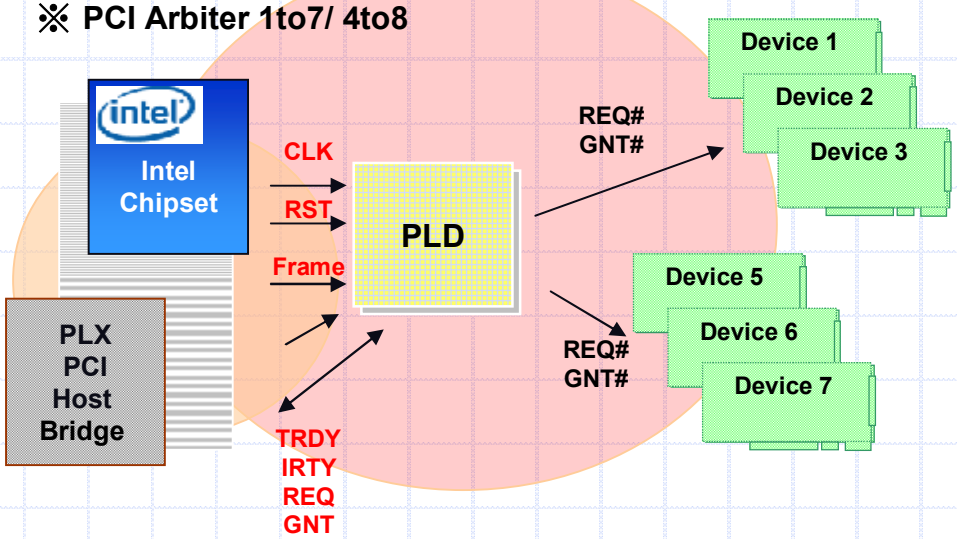
※ CANBus Solution



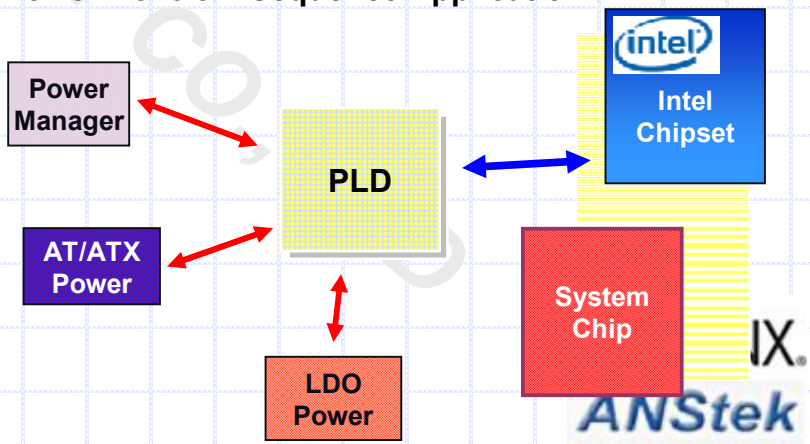
※ PCI Target Device (DIO/Motion/NVRAM) Card



※ PCI Arbiter 1to7/ 4to8

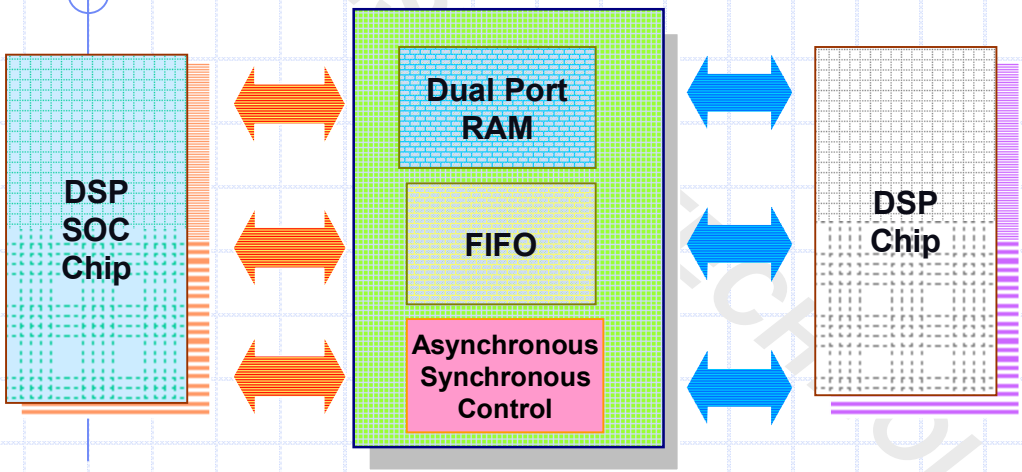


※ Power Control / Sequence Application

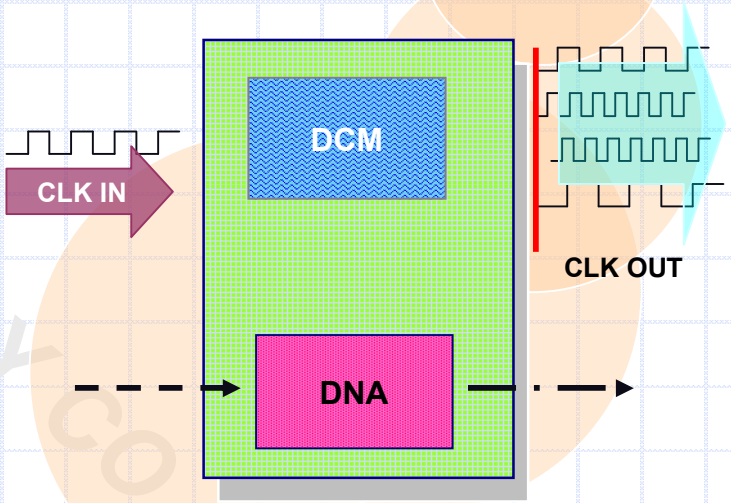


FPGA Key Feature Overview

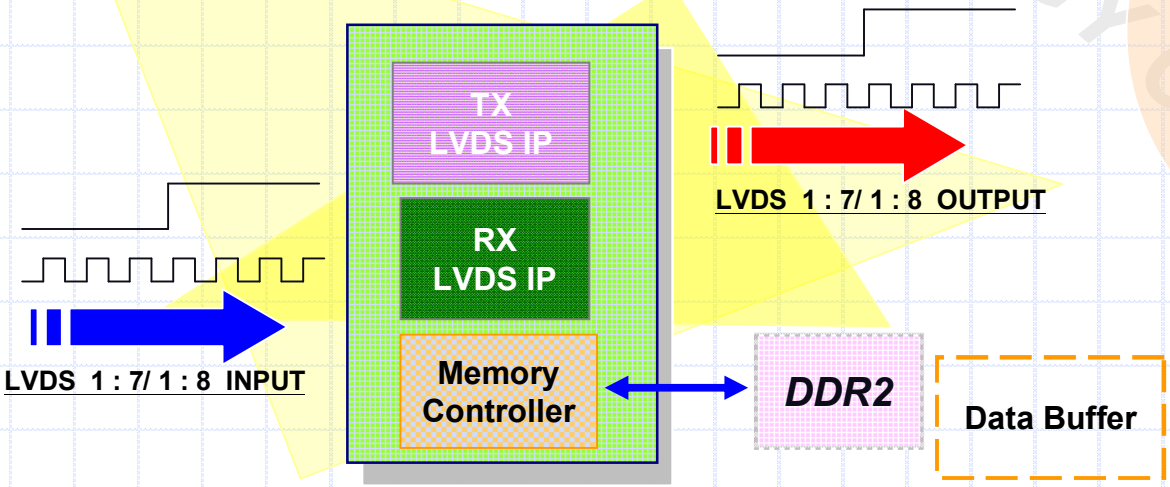
Embedded RAM App



FPFA DCM Feature



FPFA LVDS High Performances IO App



Serial Number Security Key

XILINX
ANStek