

Vivado XDC constraints



UltraFAST™ 
Design Methodology

XDC & Rodin Tcl Defined

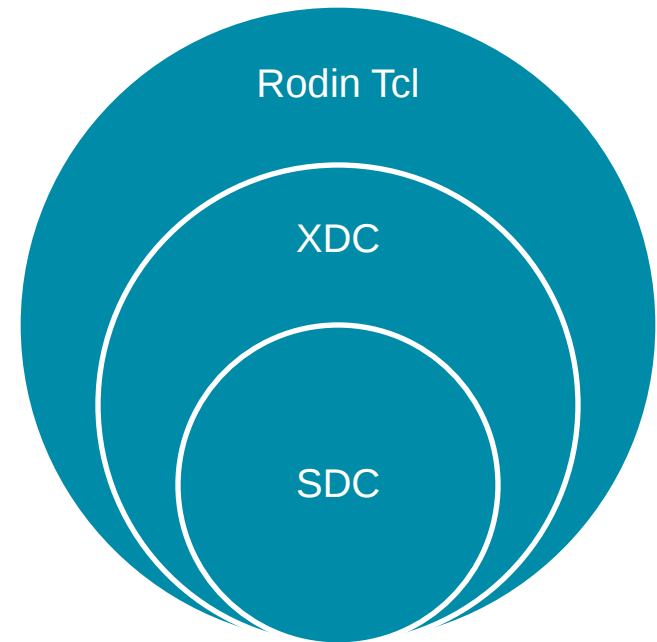
➤ SDC - Synopsys Design Constraints

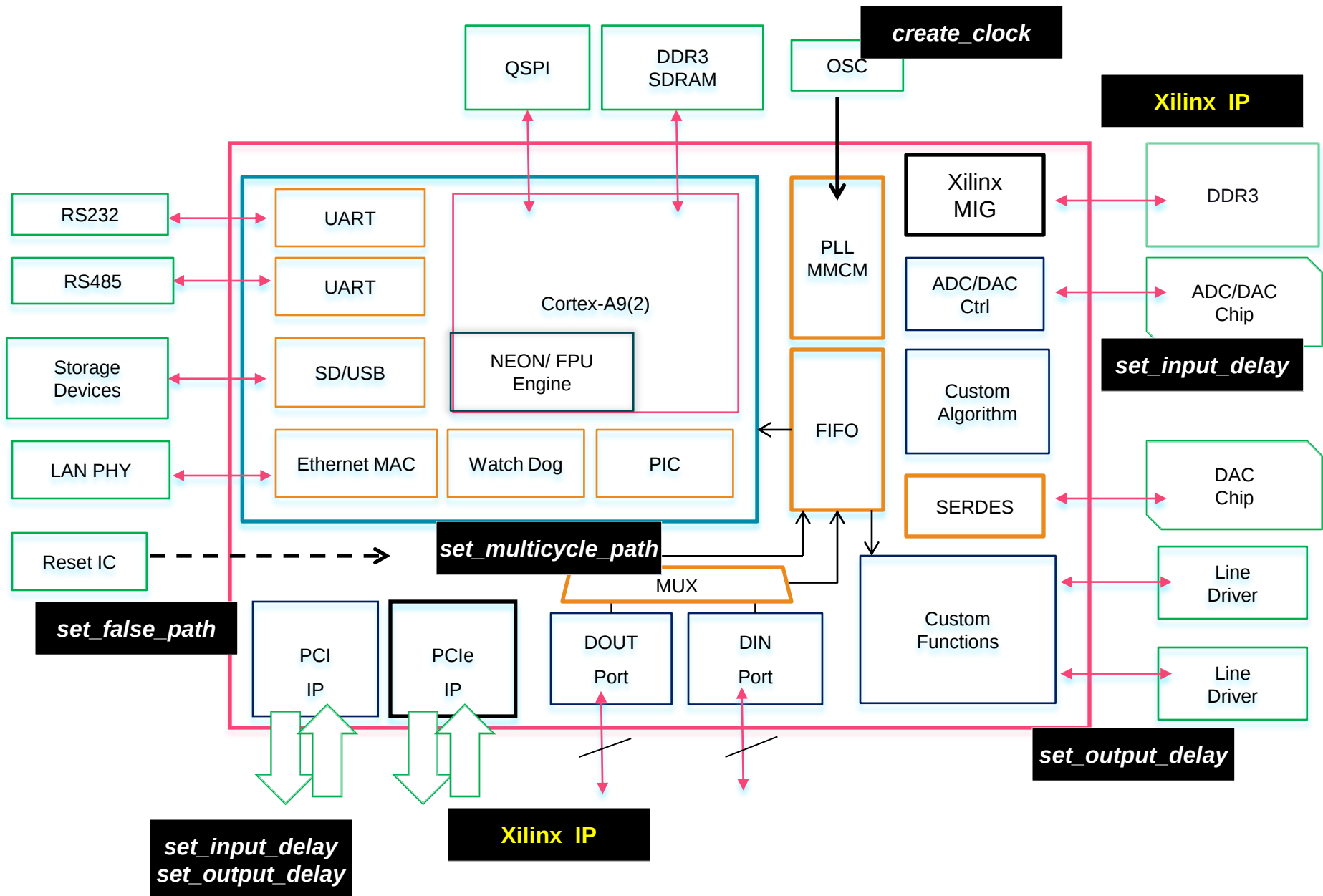
➤ XDC - Xilinx Design Constraints

- Tcl Equivalent to UCF/PCF/XCF/BCD

➤ Rodin Tcl

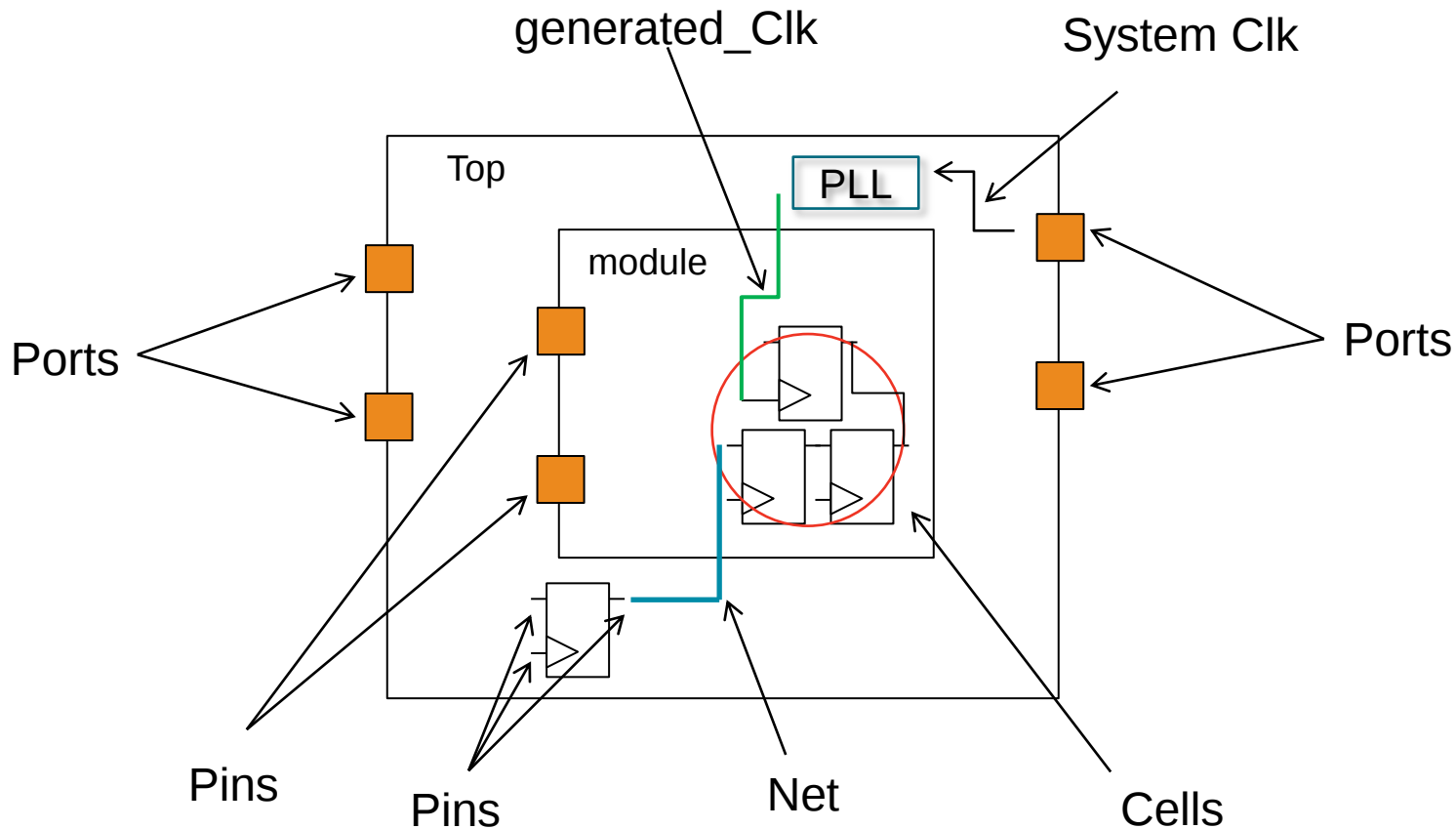
- SDC + XDC
 - Xilinx commands
 - Project, compilation, report,...
 - Xilinx objects
 - Netlist, device, timing, project,...
 - General Tcl (8.5)
 - List-related commands are overloaded to support primary objects, unlike Synopsys and Altera
 - Primary objects can directly be used with general commands, unlike Synopsys and Altera
- => Improved Ease-Of-Use!





Pins and Ports

- Once instanced, ports of a module become pins of a cell
- `get_ports` returns only top level IO ports of the design



Tcl commands in an XDC file

► Commands allowed in an XDC file

add_cells_to_pblock	get_libs	list_property_value	set_delay_model
all_clocks	get_nets	llength	set_disable_timing
all_cpus	get_package_pins	lrange	set_dont_touch_network
all_dsps	get_param	lrepeat	set_false_path
all_fanin	get_parts	lreplace	set_hierarchy_separator
all_fanout	get_path_groups	lreverse	set_input_delay
all_hsios	get_pblocks	lsearch	set_input_jitter
all_inputs	get_pins	lset	set_load
all_outputs	get_ports	lsort	set_logic_dc
all_rams	get_primitives	puts	set_logic_one
all_registers	get_property	regexp	set_logic_zero
array	get_sites	regsub	set_max_delay
concat	get_timing_arcs	remove_cells_from_pblock	set_max_fanout
create_clock	get_timing_paths	reset_default_switching_activity	set_max_route_layer
create_generated_clock	getenv	reset_operating_conditions	set_max_time_borrow
create_pblock	glob	reset_switching_activity	set_min_delay
delete_pblock	global	resize_pblock	set_mode
create_property	group_path	set	set_multicycle_path
get_attribute	incr	set_attribute	set_operating_conditions
get_cells	join	set_case_analysis	set_output_delay
get_clocks	lappend	set_clock_gating	set_param
get_debug_cores	lassign	set_clock_gating_check	set_parameter
get_debug_ports	lindex	set_clock_groups	set_propagated_clock
get_generated_clocks	linsert	set_clock_latency	set_property
get_hierarchy_separator	list	set_clock_sense	set_speed_grade
get_interfaces	list_attribute	set_clock_transition	set_switching_activity
get_iobanks	list_attribute_value	set_clock_uncertainty	set_system_jitter
get_lib_cells	list_param	set_data_check	set_units
get_lib_pins	list_property	set_default_switching_activity	read_xdc
			config_timing_analysis

UCF to XDC Mapping

Table 3-1, UCF to XDC Mapping, shows the main mapping between UCF constraints to XDC commands.

Table 3-1: UCF to XDC Mapping

UCF	SDC
TIMESPEC PERIOD	create_clock create_generated_clock
OFFSET = IN <x> BEFORE <clk>	set_input_delay
OFFSET = OUT <x> BEFORE <clk>	set_output_delay
FROM:TO "TS_"*2	set_multicycle_path
FROM:TO	set_max_delay
TIG	set_false_path
NET "clk_p" LOC = AD12	set_property LOC AD12 [get_ports clk_p]
NET "clk_p" IOSTANDARD = LVDS	set_property IOSTANDARD LVDS [get_ports clk_p]

[ug903-vivado-using-constraints.pdf](#)

Timing Constraints

Timing constraints must be passed to the synthesis engine by means of one or more XDC files. Only the following constraints related to setup analysis have any real impact on synthesis results:

- create_clock
- create_generated_clock
- set_input_delay
- set_output_delay
- set_clock_groups
- set_false_path
- set_max_delay
- set_multicycle_path

[ug911-vivado-migration.pdf](#)

Between Groups

UCF Example `TIMESPEC TS_TIG = FROM reset_ff TO FFS TIG;`

XDC Example Manual conversion is required. Construct a `set_false_path` that covers the desired paths.

By Net

UCF Example `NET reset TIG;`

XDC Example `set_false_path -through [get_nets reset]`
A better approach is to find the primary reset port and use:
`set_false_path -from [get_ports reset_port]`

By Instance

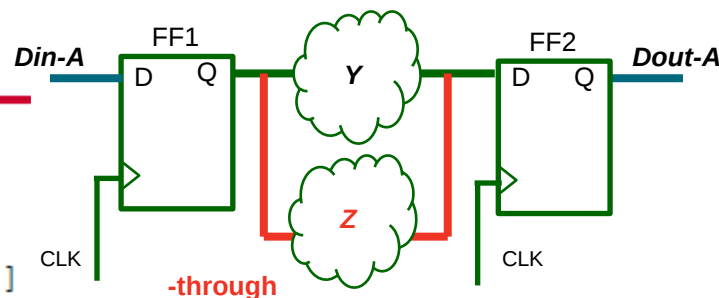
UCF Example `INST reset TIG;`

XDC Example `set_false_path -from [get_cells reset]`
`set_false_path -through [get_cells reset]`
`set_false_path -to [get_cells reset]`

By Pin

UCF Example `PIN ff.d TIG;`

XDC Example `set_false_path -to [get_pins ff/D]`
`set_false_path -from [get_pins ff/C]`
`set_false_path -through [get_pins lut/I0]`

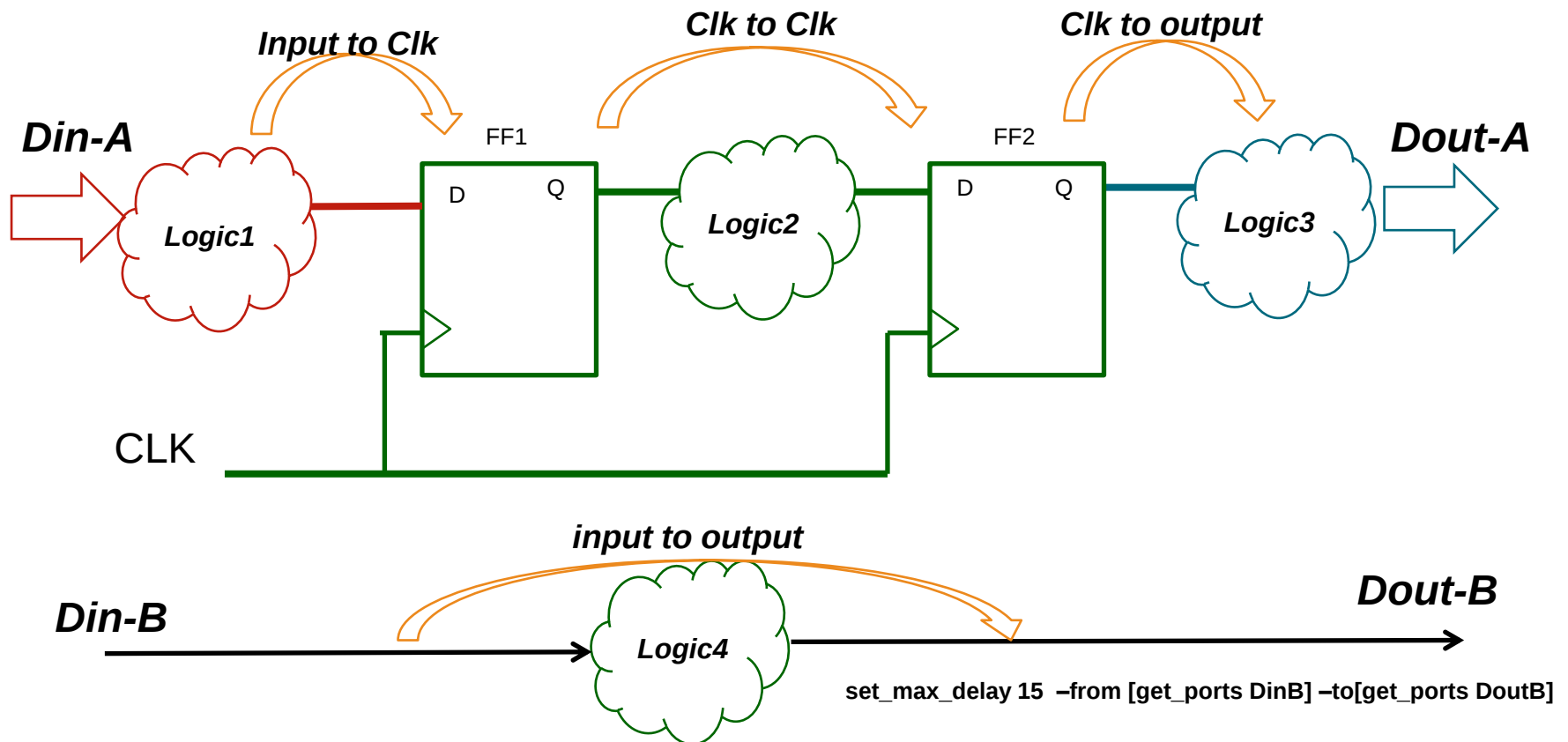


ug911-vivado-migration.pdf

Timing Paths

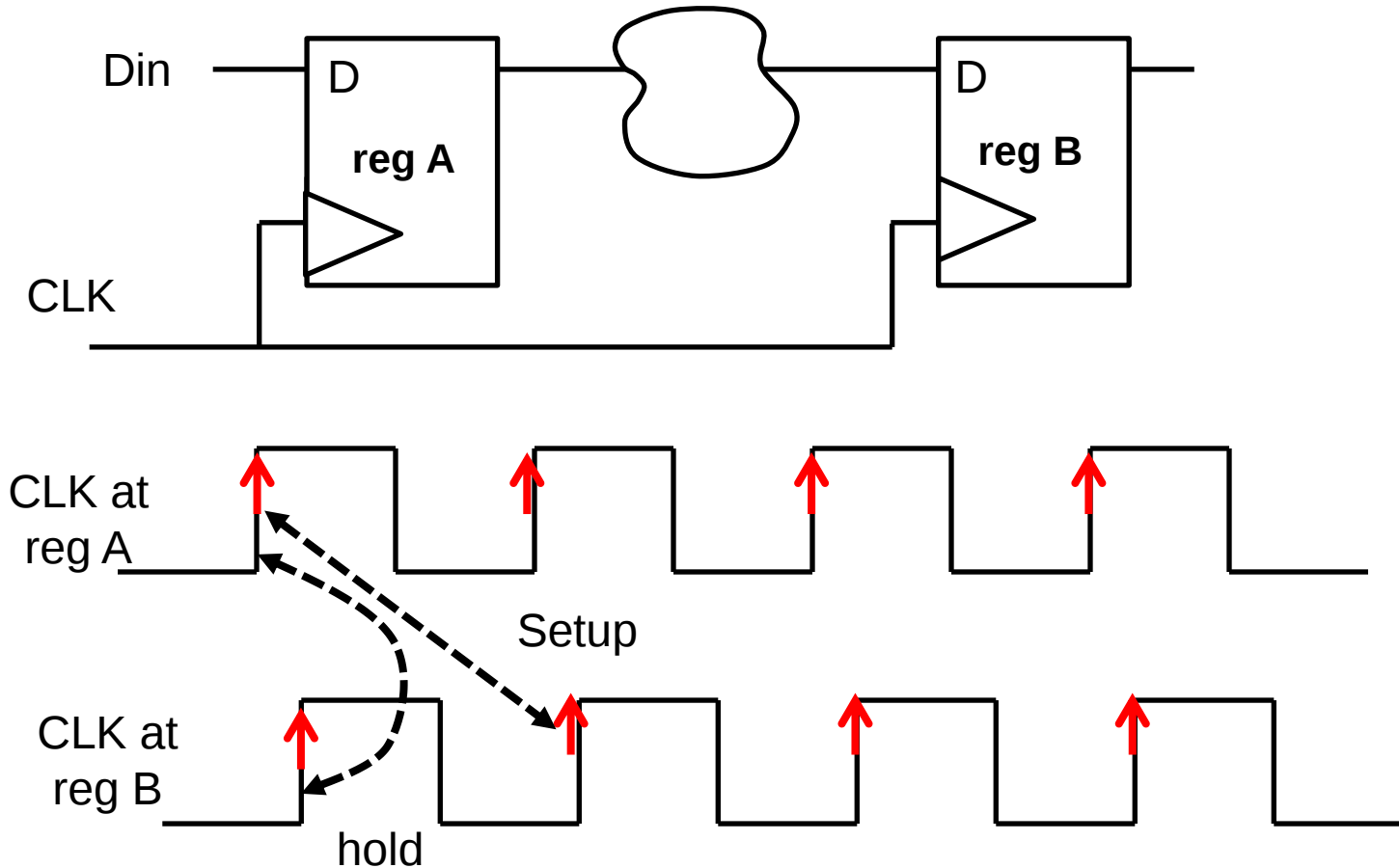
■ These basic timing paths can apply to:

- ◆ A module within an ASIC/FPGA
- ◆ A whole ASIC/FPGA
- ◆ A system with multiple chips



Timing Analysis: Setup/Hold Check

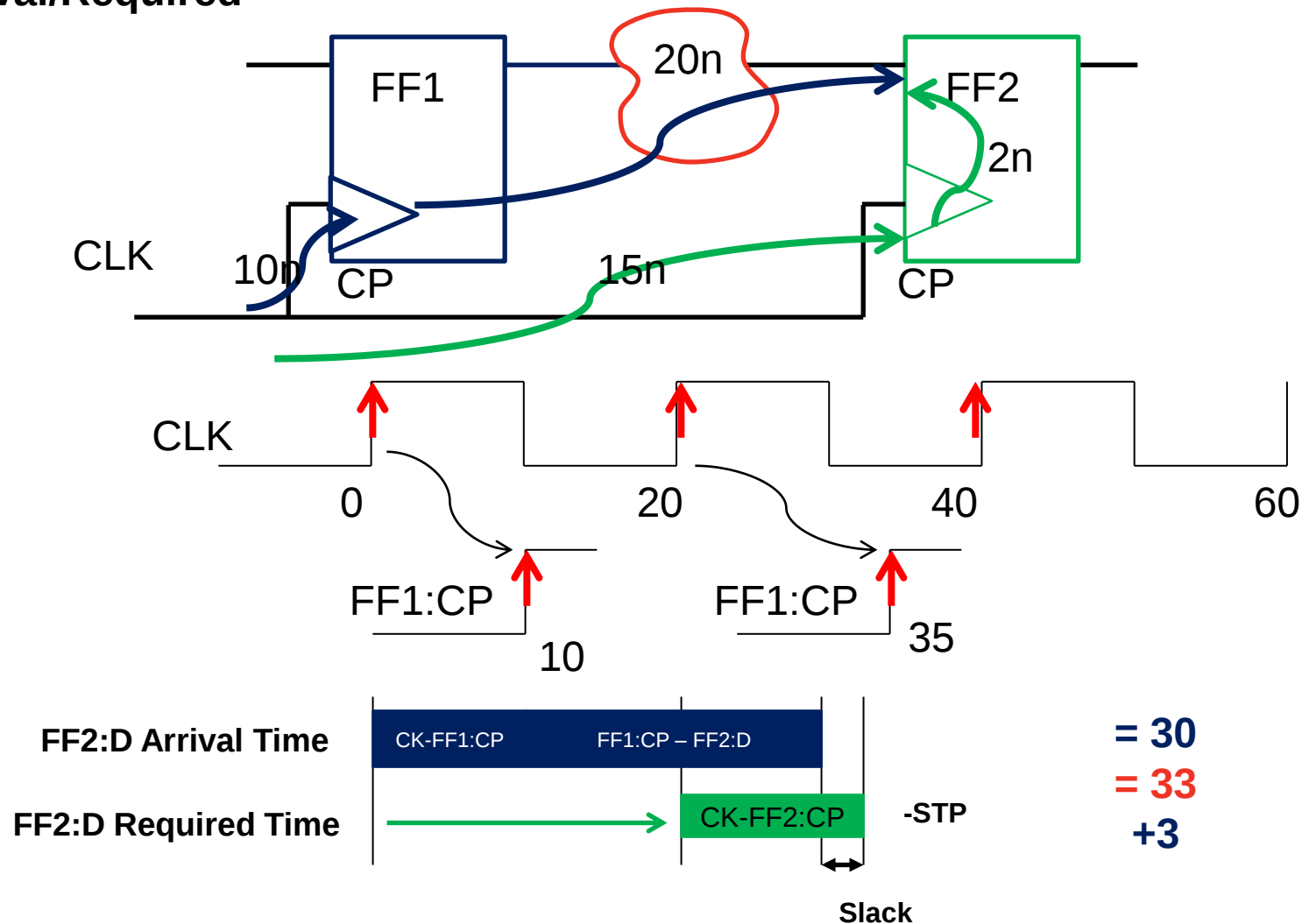
■ Create Clock: reg-to-reg requirement



Single-cycle timing relationship

Setup Check

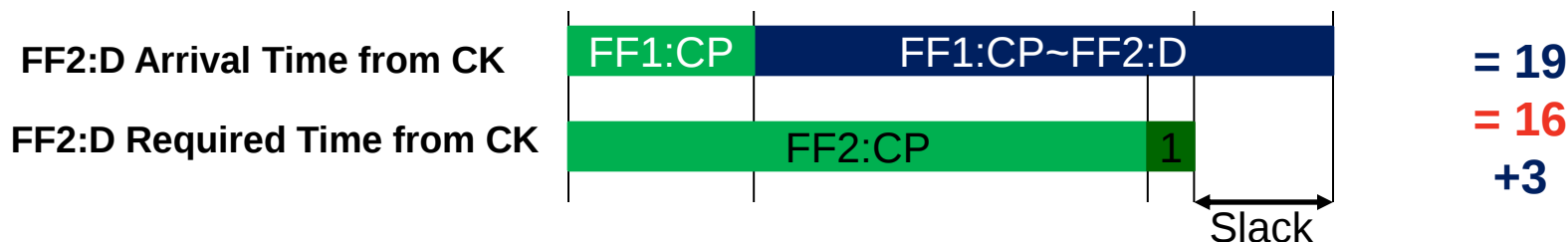
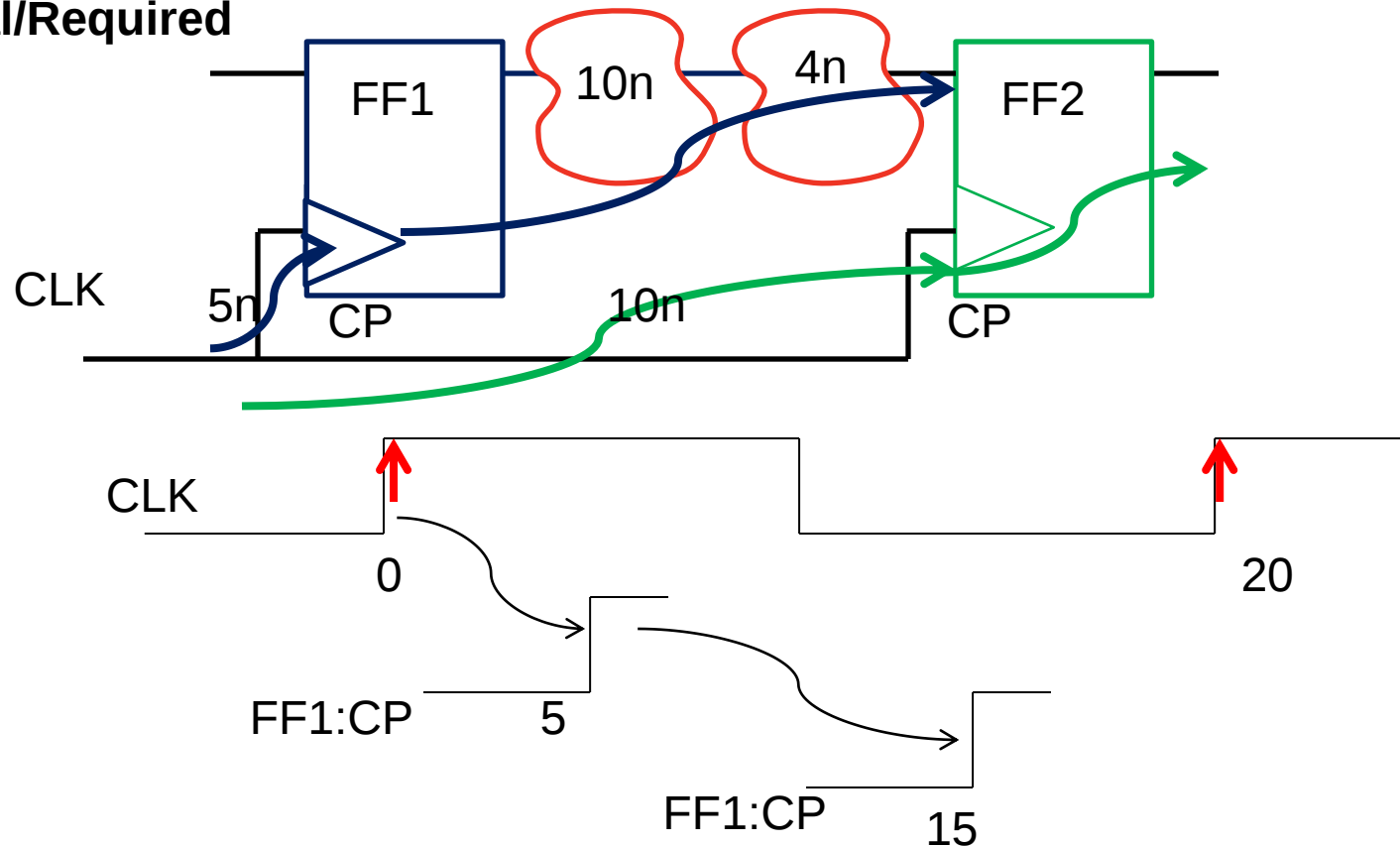
Arrival/Required



Slack = Required_time – Arrival_time (Violation if < 0)

Hold Check

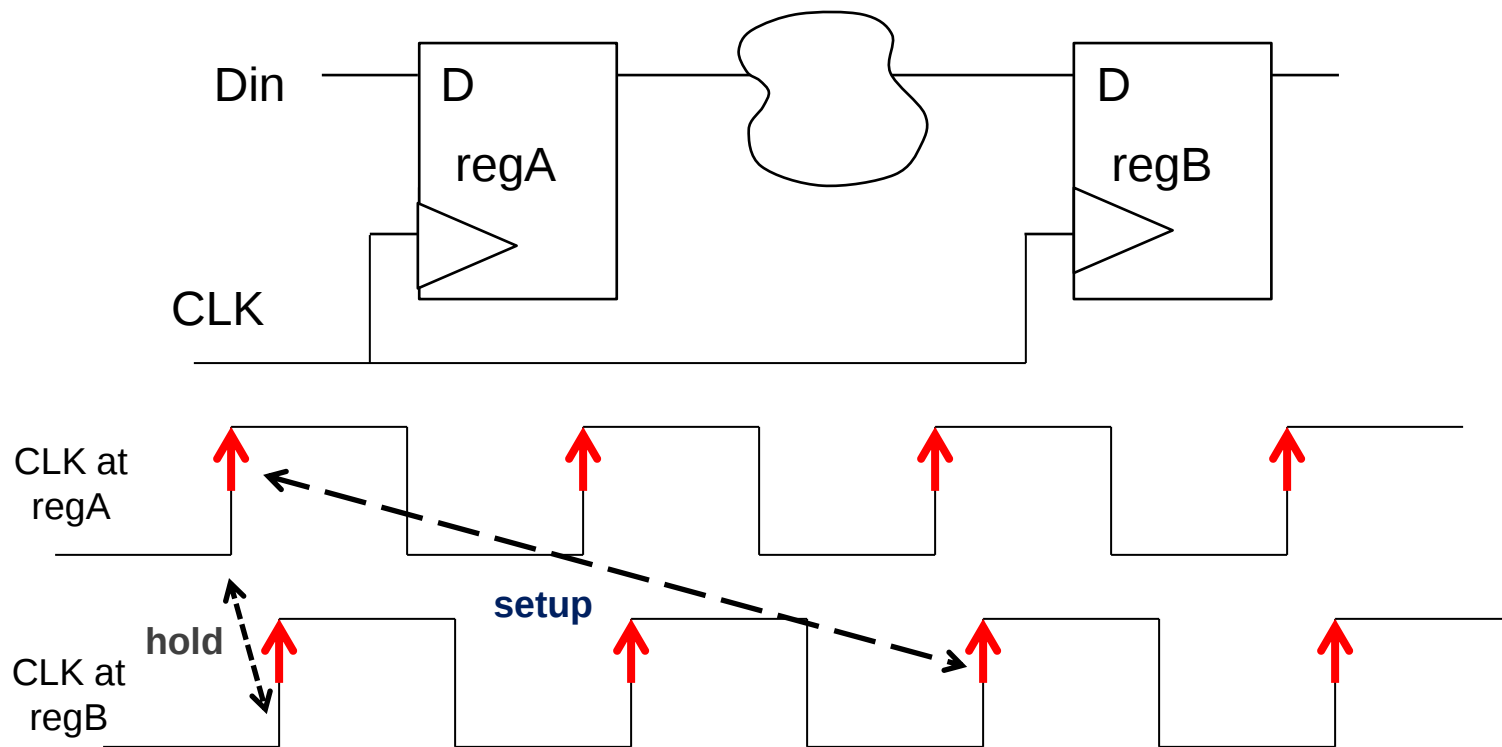
Arrival/Required



Slack = ArrivalTime – RequiredTime (Violation if < 0)

Timing Analysis: Multi-cycle

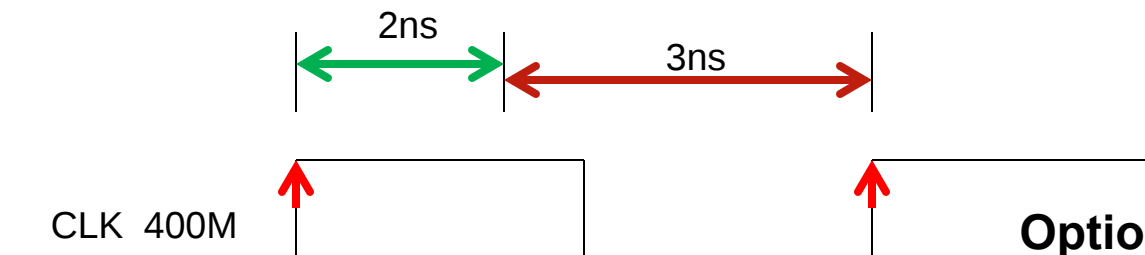
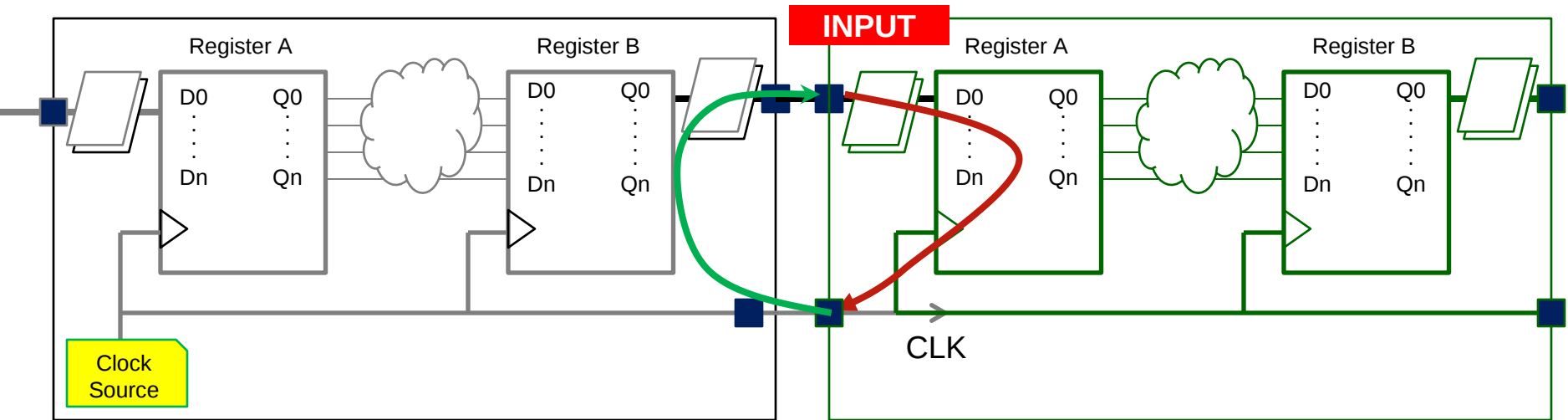
- `set_multicycle_path -from [get_cells {1_reg[*]}] -to [get_cells {2_reg[*]}] 2`
- `set_multicycle_path -from [get_cells {1_reg[*]}] -to [get_cells {2_reg[*]}] -hold 1`



Multi-cycle timing relationship

Input Delay Constraints

■ Captures External Setup/Hold Requirements

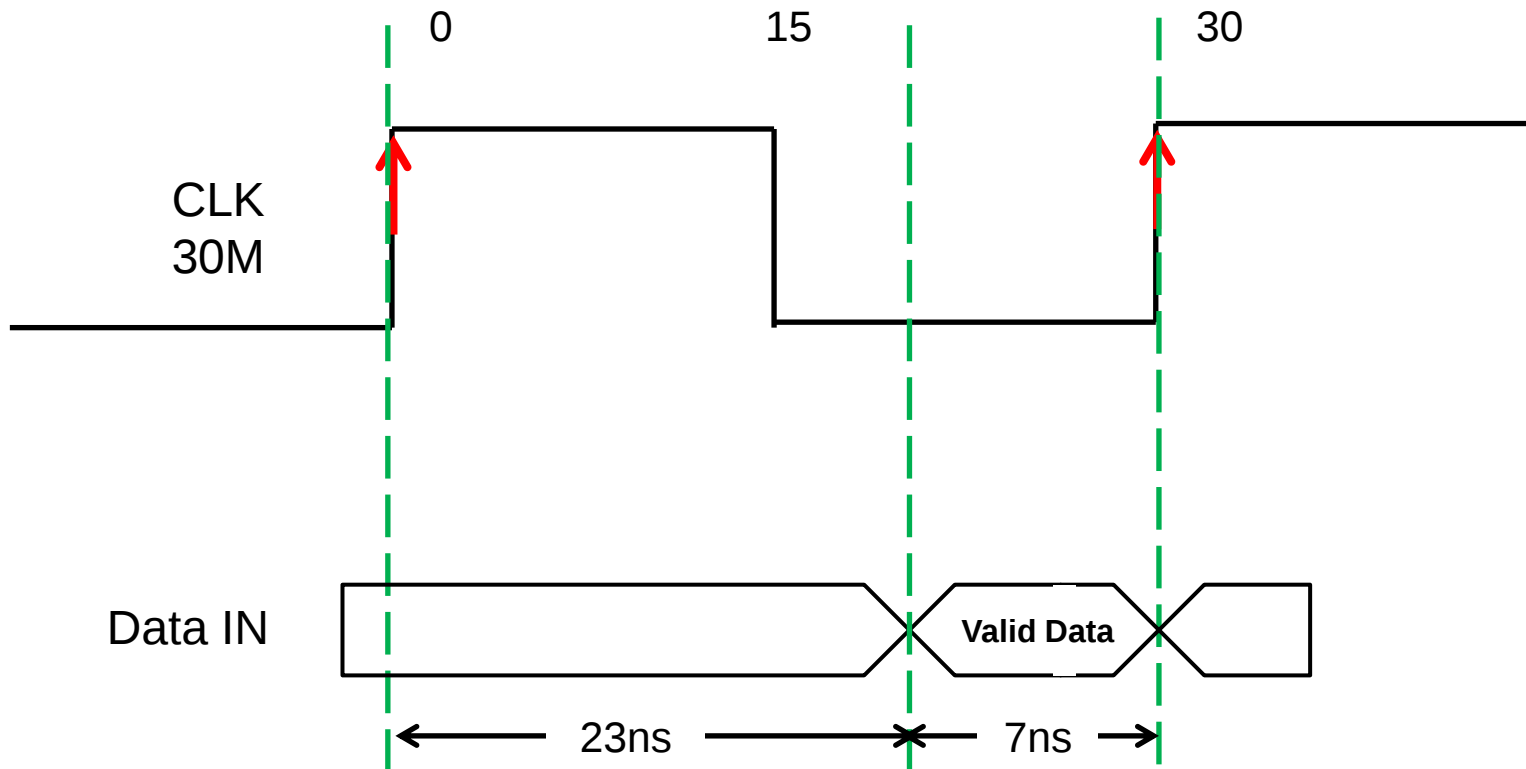


Option “-min” for hold check
Option “-max” for setup check

XDC: set_input_delay 2.0 -clock CK {IN}

Constraining Designs

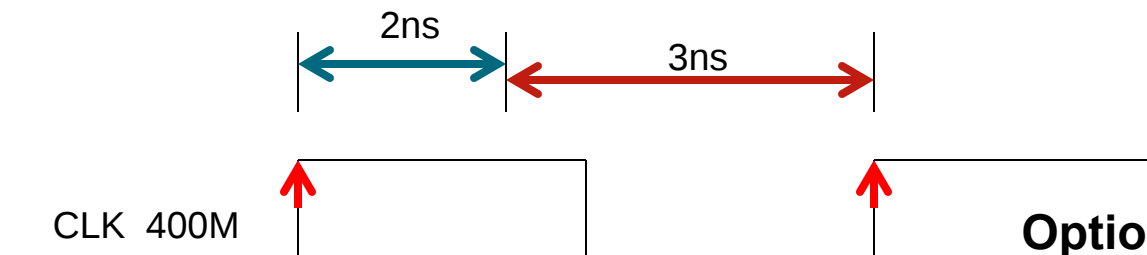
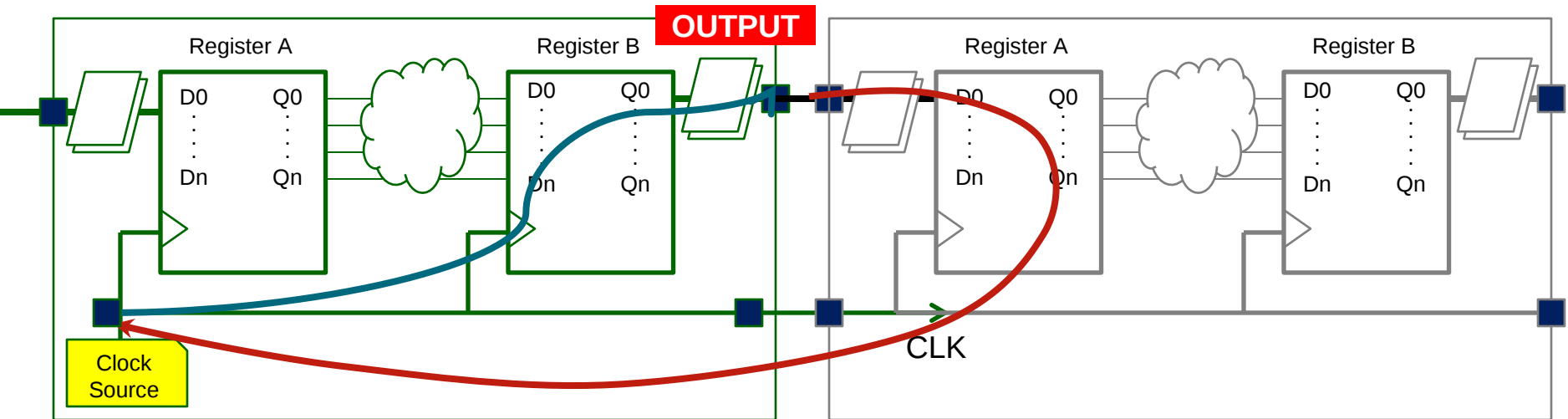
- Set Input Delay: setup/hold requirements



```
set_input_delay -max 23.0 -min 0.0 -clock clk {datain}
```

Output Delay Constraint

■ Captures Clock-to-Out Requirements

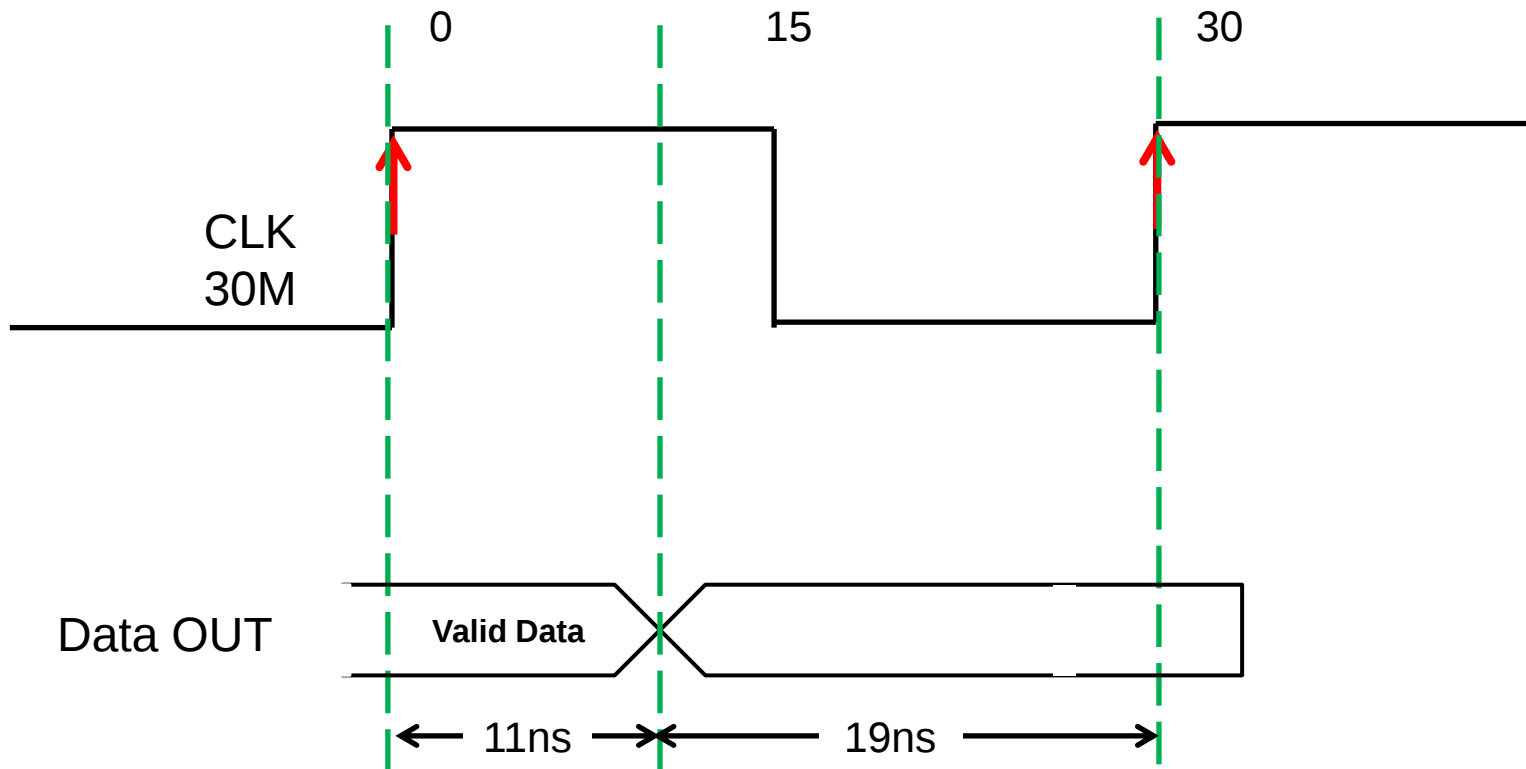


Option “-min” for hold check
Option “-max” for setup check

XDC: set_output_delay 3.0 -clock CK {OUT}

Constraining Designs

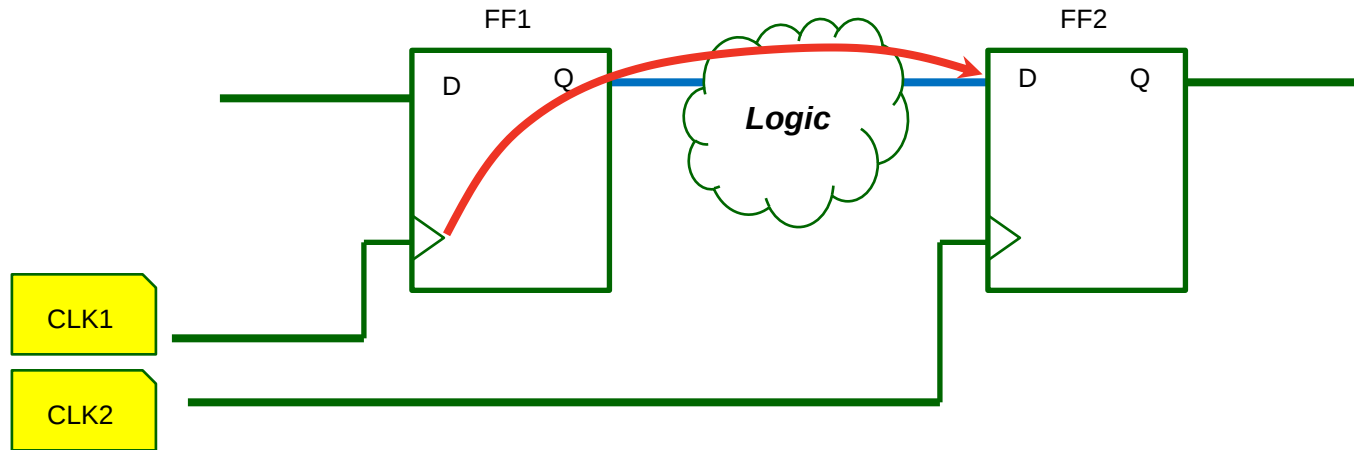
- Set output Delay: Clock-to-out requirements



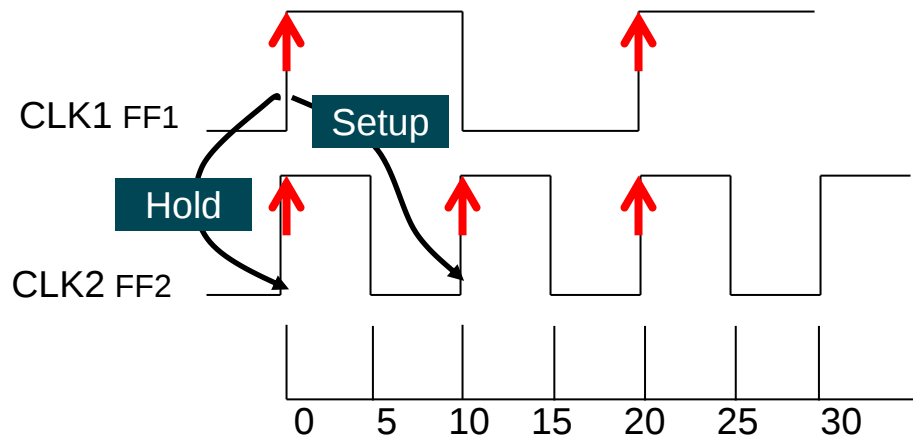
```
set_output_delay -max 19.0 -clock clk {dataout}
```

Cross-Domain Analysis

■ Study over the Least Common Multiplier



```
XDC : creat_clock -period 20 -waveform { 0 10} CLK1  
XDC : creat_clock -period 10 -waveform { 0 5 } CLK2
```



Vivado Timing Edit

project_1 - [F:/ANSTEK_Training/vivado_xdc/project_1/project_1.xpr] - Vivado 2013.3

File Edit Flow Tools Window Layout View Help

IO Planning

Synthesis and Implementation Out-of-Date [more info](#)

Synthesized Design - xc7k70tbg676-1 (active)

Package x Device x pcie_7x_0-PCIE_X0Y0.xdc x Timing Constraints x

Top_jeollee

Nets (495)

Leaf Cells (209)

MIG_Ctrl (exa)

PCI_Slave (PC)

PCle_gen2x4

Inputs (6)

Outputs (1)

Create Clock

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File	Scoped Cell	Cu
1	pcie_7x_0_bx...	10.000			☐	[get_pins PCle_gen2x4/pci...	pcie_7x_0-PCIE_X0Y0.xdc	PCle_gen2x4/pci_7x_0_i/inst	
4	sys_clk	5.000			☒	[get_ports sys_clk_p]	mig_7series_0.xdc	MIG_Ctrl/mig_7series_0	
14	pcie_clk	10.000			☐	[get_pins PCle_gen2x4/refc...	pcie_7x_0-PCIE_X0Y0.xdc		
19	sys_clk	5.000	0.000	2.500	☐	[get_ports sys_clk_p]	pcie_7x_0-PCIE_X0Y0.xdc		
22	PCICLK	30.000			☐	[get_ports PCICLK]	pcie_7x_0-PCIE_X0Y0.xdc		

Double click to create a Create Clock constraint

All Constraints

- pcie_7x_0-PCIE_X0Y0.xdc (scoped to: PCle_gen2x4/pci_7x_0_i/inst) (f:/ANSTEK_Training/vivado_xdc/project_1/project_1.srcs/sources_1/hp/pcie_7x_0/pcie_7x_0/source/pcie_7x_0-PCIE_X0Y0.xdc)
 - 1. create_clock -period 10.000 -name pcie_7x_0_boutclk_out [get_pins PCle_gen2x4/pci_7x_0_i/inst/pipe_boutclk_out]
 - 2. set_false_path -through [get_pins inst/pcie_top_i/pcie_7x_0/pcie_block_i/PLPHYLKUPN*]
 - 3. set_false_path -through [get_pins inst/pcie_top_i/pcie_7x_0/pcie_block_i/PLRECEIVEDHOTRST*]
- mig_7series_0.xdc (scoped to: MIG_Ctrl/mig_7series_0) (f:/ANSTEK_Training/vivado_xdc/project_1/project_1.srcs/sources_1/hp/mig_7series_0/mig_7series_0/user_design/constraints/mig_7series_0.xdc)
 - create_clock -period 5.000 -name sys_clk [get_ports sys_clk_p]
 - 5. set_multicycle_path -setup -from [get_cells -hier -filter (NAME =~ */mc0/mc_read_idle_r_reg)] -to [get_cells -hier -filter (NAME =~ */input_0/iserdes_dq_iserdesdq)] 6
 - 6. set_multicycle_path -hold -from [get_cells -hier -filter (NAME =~ */mc0/mc_read_idle_r_reg)] -to [get_cells -hier -filter (NAME =~ */input_0/iserdes_dq_iserdesdq)] 5
 - 7. set_false_path -through [get_pins -filter (NAME =~ */FOSC0BOUND)] -of [get_cells -hier -filter (NAME =~ */FOSC0BOUND)]

Apply Cancel

IO Ports

Name	Direction	Neg Diff Pair	Site	Fixed	Bank	I/O Std	Vcco	Vref	Drive Stren...	Slew Type	Pull Type	Off-Chip T...
All ports (215)												

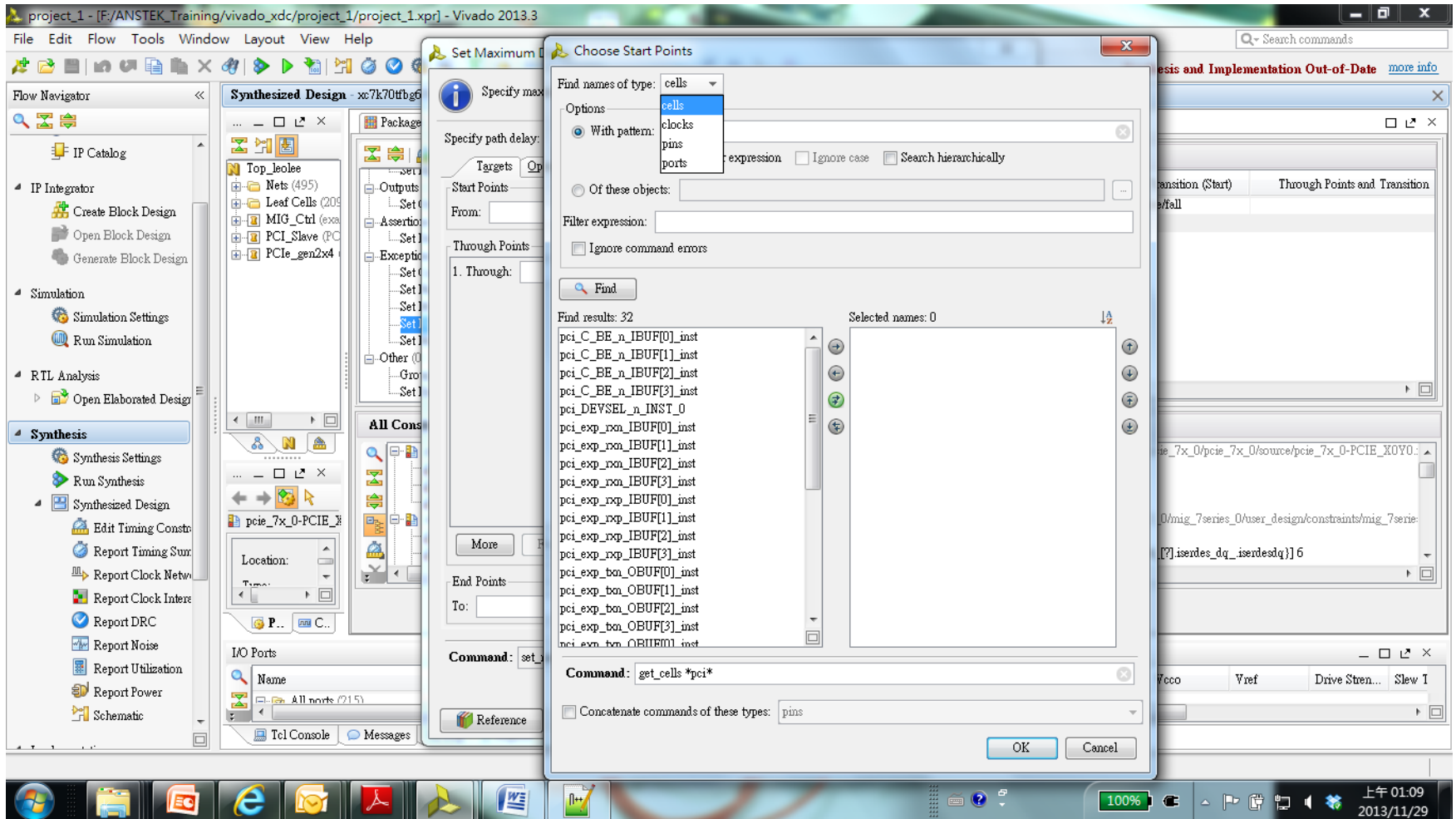
Tcl Console Messages Log Reports Design Runs Package Pins I/O Ports

XDC Command: create_clock -period 5.000 -name sys_clk [get_ports sys_clk_p]

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Vivado GUI Interface

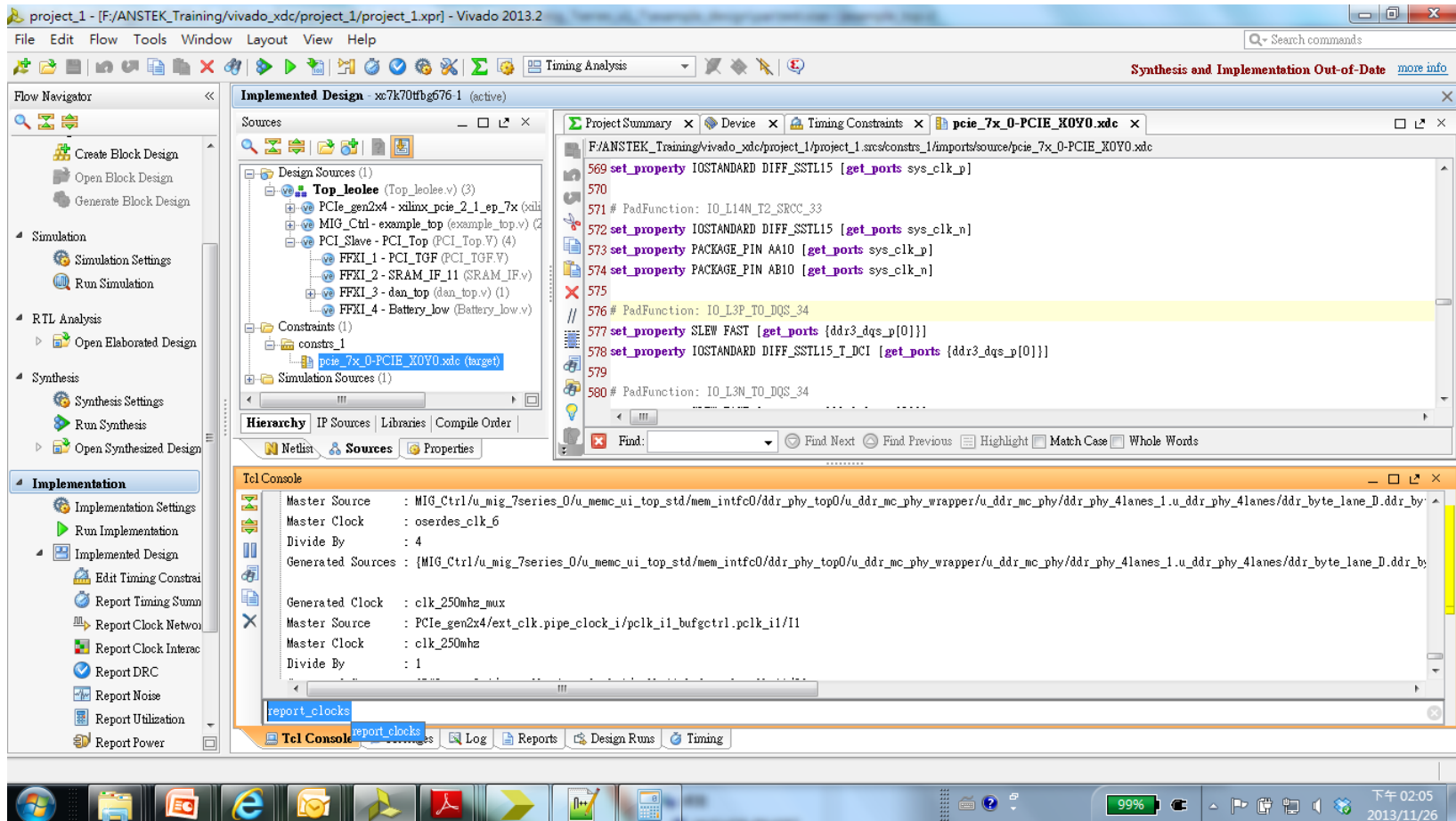
Cells/Clock/Pins/Ports

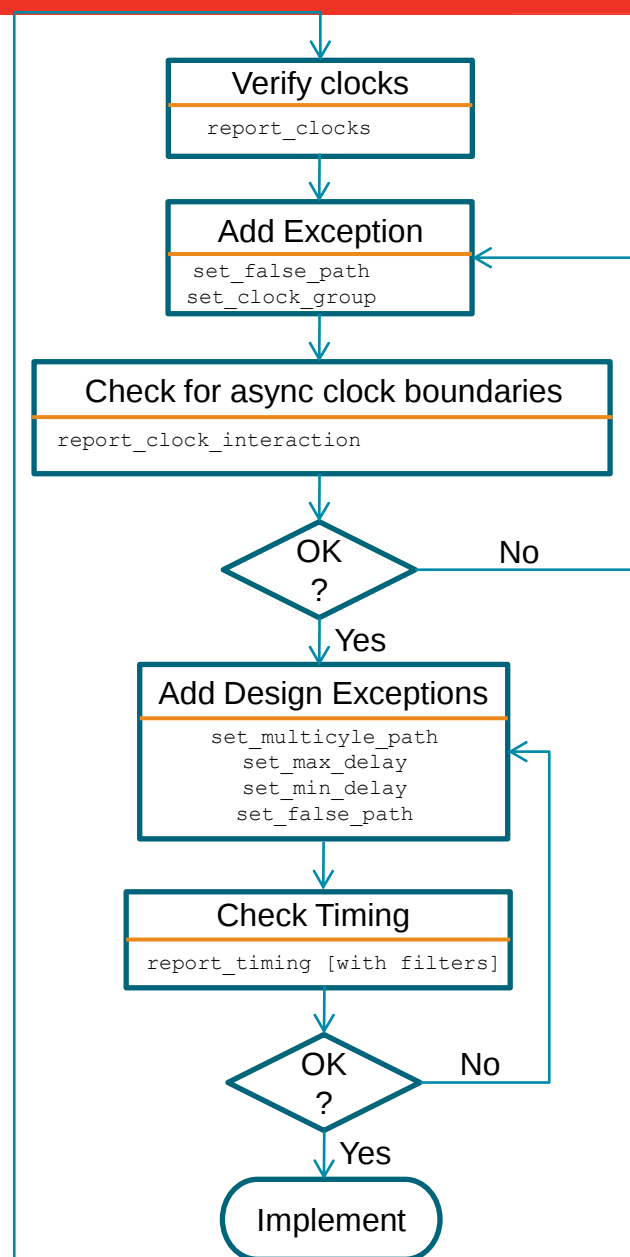
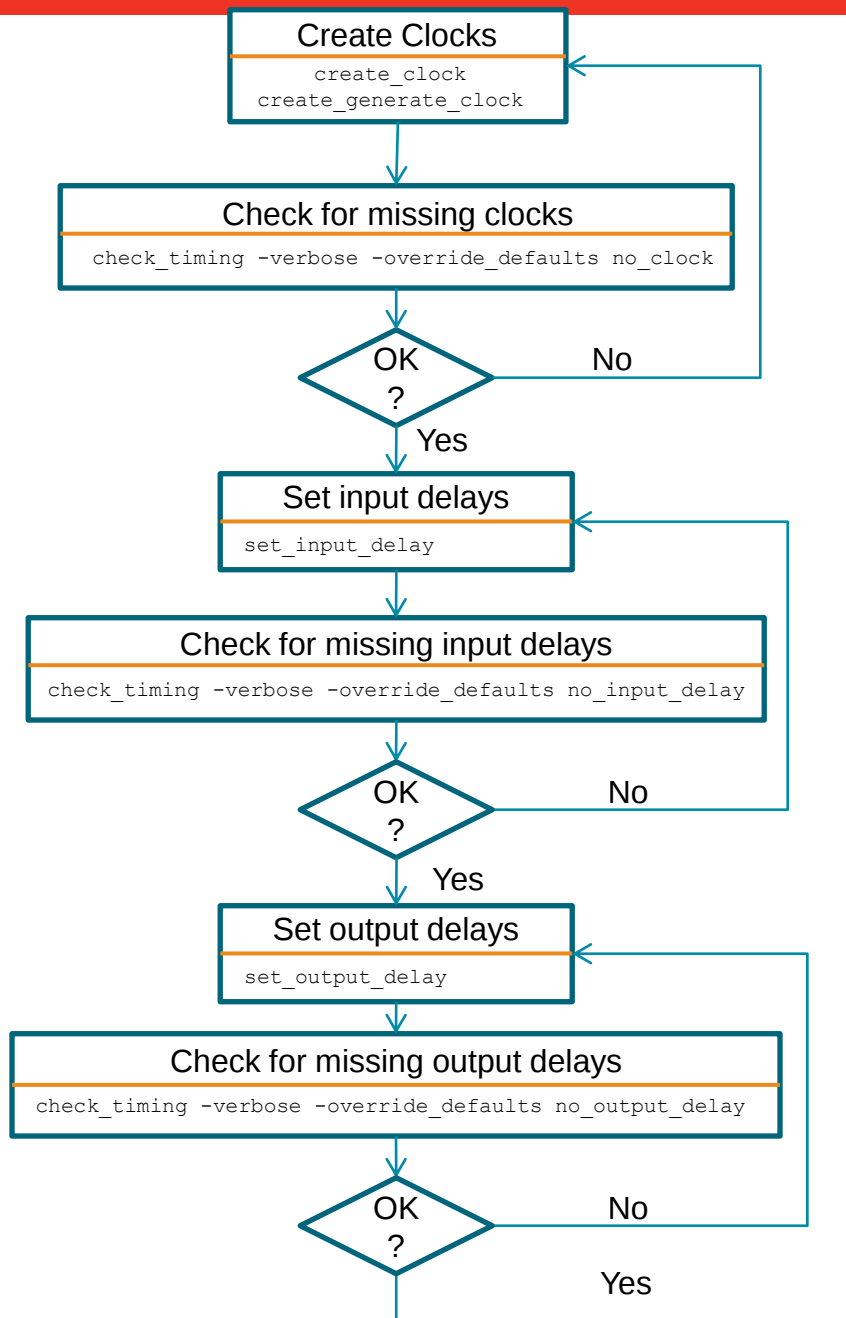


TCL Command Windows

% help –category <name>

- gives list and brief description of commands in that category





More Info

- [***ISE to Vivado Design Suite Migration Guide***](#)
- [***Migrating UCF Constraints to XDC – YouTube***](#)
- [***Vivado Design Suite Tcl Command Reference Guide***](#)
- [***Vivado Design Suite User Guide / Using Constraints***](#)
- [***Vivado Design Suite Properties Reference Guide***](#)
- [***Vivado Design Suite User Guide Programming and Debugging***](#)