VIVADO
Productivity. Multiplied.

XILINX
ALL PROGRAMMABLE™

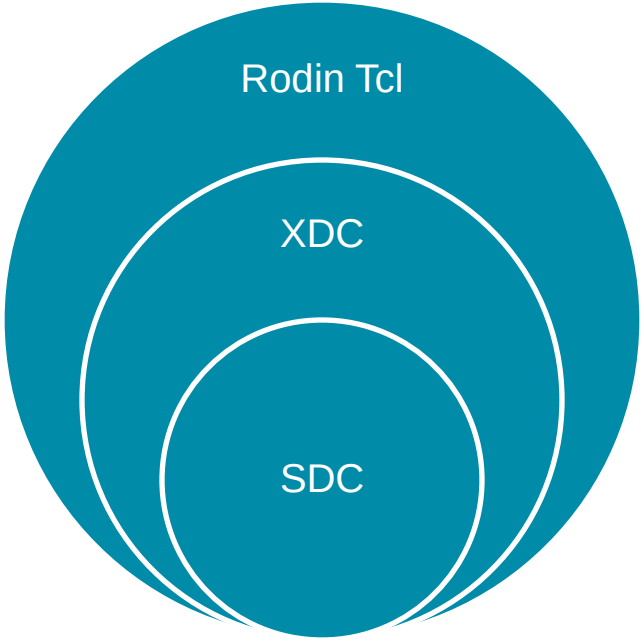
Vivado XDC constraints

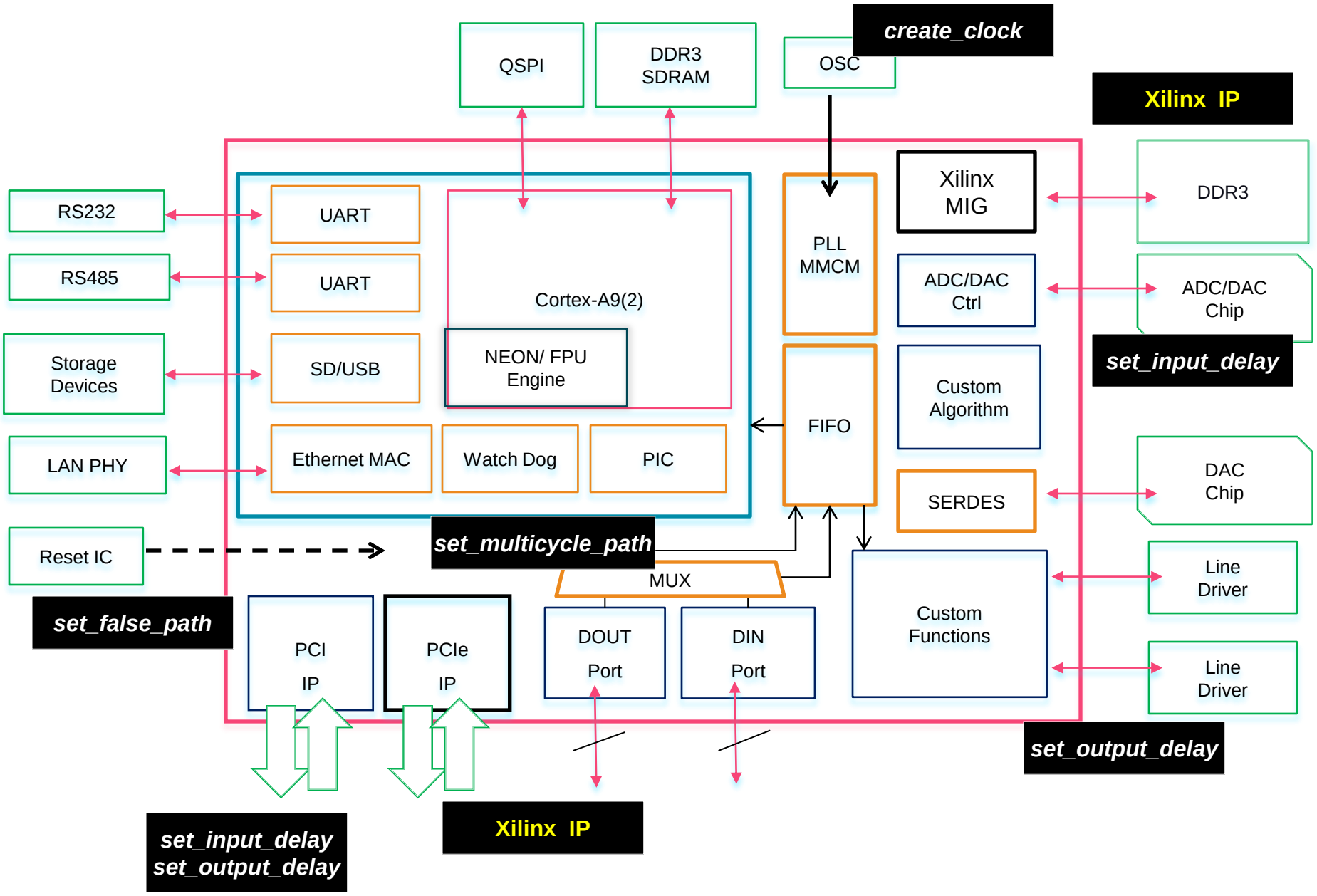
UltraFAST™
Design Methodology

XDC & Rodin Tcl Defined

- **SDC - Synopsys Design Constraints**
- **XDC - Xilinx Design Constraints**
  - Tcl Equivalent to UCF/PCF/XCF/BCD
- **Rodin Tcl**
  - SDC + XDC
  - Xilinx commands
    - Project, compilation, report,…
  - Xilinx objects
    - Netlist, device, timing, project,…
  - General Tcl (8.5)
    - List-related commands are overloaded to support primary objects, unlike Synopsys and Altera
    - Primary objects can directly be used with general commands, unlike Synopsys and Altera

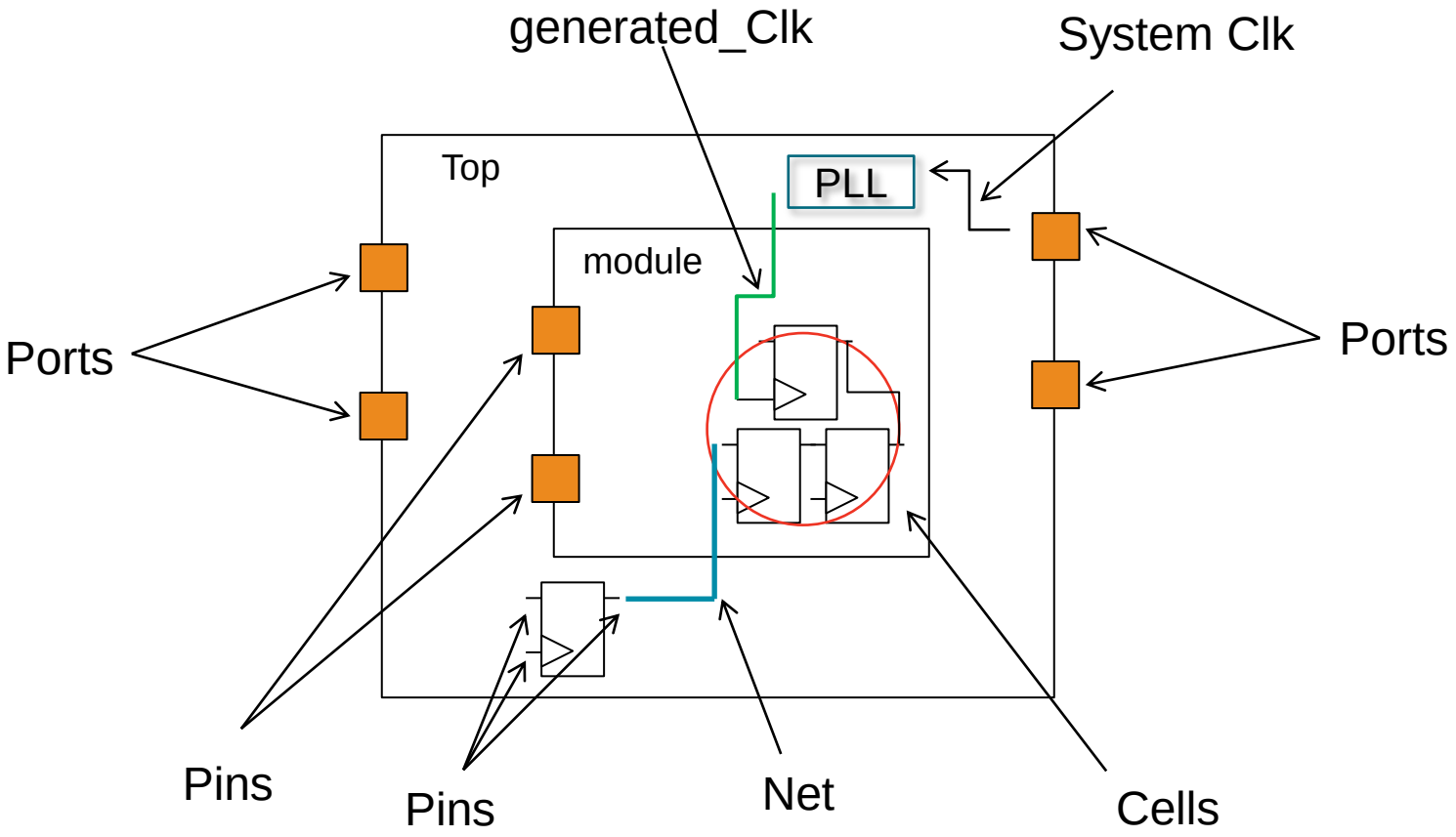
    => Improved Ease-Of-Use!





Pins and Ports

- Once instanced, ports of a module become pins of a cell
- **get_ports** returns only top level IO ports of the design



Tcl commands in an XDC file

Commands allowed in an XDC file

add_cells_to_pblock
all_clocks
all_cpus
all_dsps
all_fanin
all_fanout
all_hsios
all_inputs
all_outputs
all_rams
all_registers
array
concat
create_clock
create_generated_clock
create_pblock
delete_pblock
create_property
get_attribute
get_cells
get_clocks
get_debug_cores
get_debug_ports
get_generated_clocks
get_hierarchy_separator
get_interfaces
get_iobanks
get_lib_cells
get_lib_pins
get_libs
get_nets
get_package_pins
get_param
get_parts
get_path_groups
get_pblocks
get_pins
get_ports
get_primitives
get_property
get_sites
get_timing_arcs
get_timing_paths
getenv
glob
global
group_path
incr
join
lappend
lassign
lindex
linsert
list
list_attribute
list_attribute_value
list_param
list_property
list_property_value
llength
lrange
lrepeat
lreplace
lreverse
lsearch
lset
lsort
puts
regexp
regsub
remove_cells_from_pblock
reset_default_switching_activity
reset_operating_conditions
reset_switching_activity
resize_pblock
set
set_attribute
set_case_analysis
set_clock_gating
set_clock_gating_check
set_clock_groups
set_clock_latency
set_clock_sense
set_clock_transition
set_clock_uncertainty
set_data_check
set_default_switching_activity
set_delay_model
set_disable_timing
set_dont_touch_network
set_false_path
set_hierarchy_separator
set_input_delay
set_input_jitter
set_load
set_logic_dc
set_logic_one
set_logic_zero
set_max_delay
set_max_fanout
set_max_route_layer
set_max_time_borrow
set_min_delay
set_mode
set_multicycle_path
set_operating_conditions
set_output_delay
set_param
set_parameter
set_propagated_clock
set_property
set_speed_grade
set_switching_activity
set_system_jitter
set_units
read_xdc
config_timing_analysis

UCF to XDC Mapping

Table 3-1, UCF to XDC Mapping, shows the main mapping between UCF constraints to XDC commands.

Table 3-1: **UCF to XDC Mapping**

UCF	SDC
TIMESPEC PERIOD	create_clock create_generated_clock
OFFSET = IN <x> BEFORE <clk>	set_input_delay
OFFSET = OUT <x> BEFORE <clk>	set_output_delay
FROM:TO "TS_"*2	set_multicycle_path
FROM:TO	set_max_delay
TIG	set_false_path
NET "clk_p" LOC = AD12	set_property LOC AD12 [get_ports clk_p]
NET "clk_p" IOSTANDARD = LVDS	set_property IOSTANDARD LVDS [get_ports clk_p]

ug903-vivado-using-constraints.pdf

Timing Constraints

Timing constraints must be passed to the synthesis engine by means of one or more XDC files. Only the following constraints related to setup analysis have any real impact on synthesis results:

- create_clock
- create_generated_clock
- set_input_delay
- set_output_delay
- set_clock_groups
- set_false_path
- set_max_delay
- set_multicycle_path

ug911-vivado-migration.pdf

Between Groups

UCF Example	`TIMESPEC TS_TIG = FROM reset_ff TO FFS TIG;`
XDC Example	Manual conversion is required. Construct a `set_false_path` that covers the desired paths.

By Net

UCF Example	`NET reset TIG;`

XDC Example	`set_false_path -through [get_nets reset]`
	A better approach is to find the primary reset port and use:
	`set_false_path -from [get_ports reset_port]`

By Instance

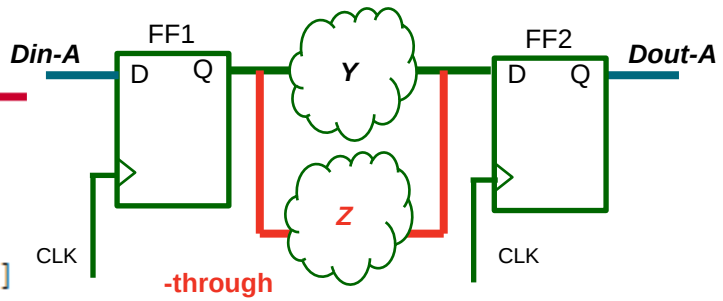
UCF Example	`INST reset TIG;`

XDC Example	`set_false_path -from [get_cells reset]`
	`set_false_path -through [get_cells reset]`
	`set_false_path -to [get_cells reset]`

By Pin

UCF Example	`PIN ff.d TIG;`

XDC Example	`set_false_path -to [get_pins ff/D]`
	`set_false_path -from [get_pins ff/C]`
	`set_false_path -through [get_pins lut/I0]`



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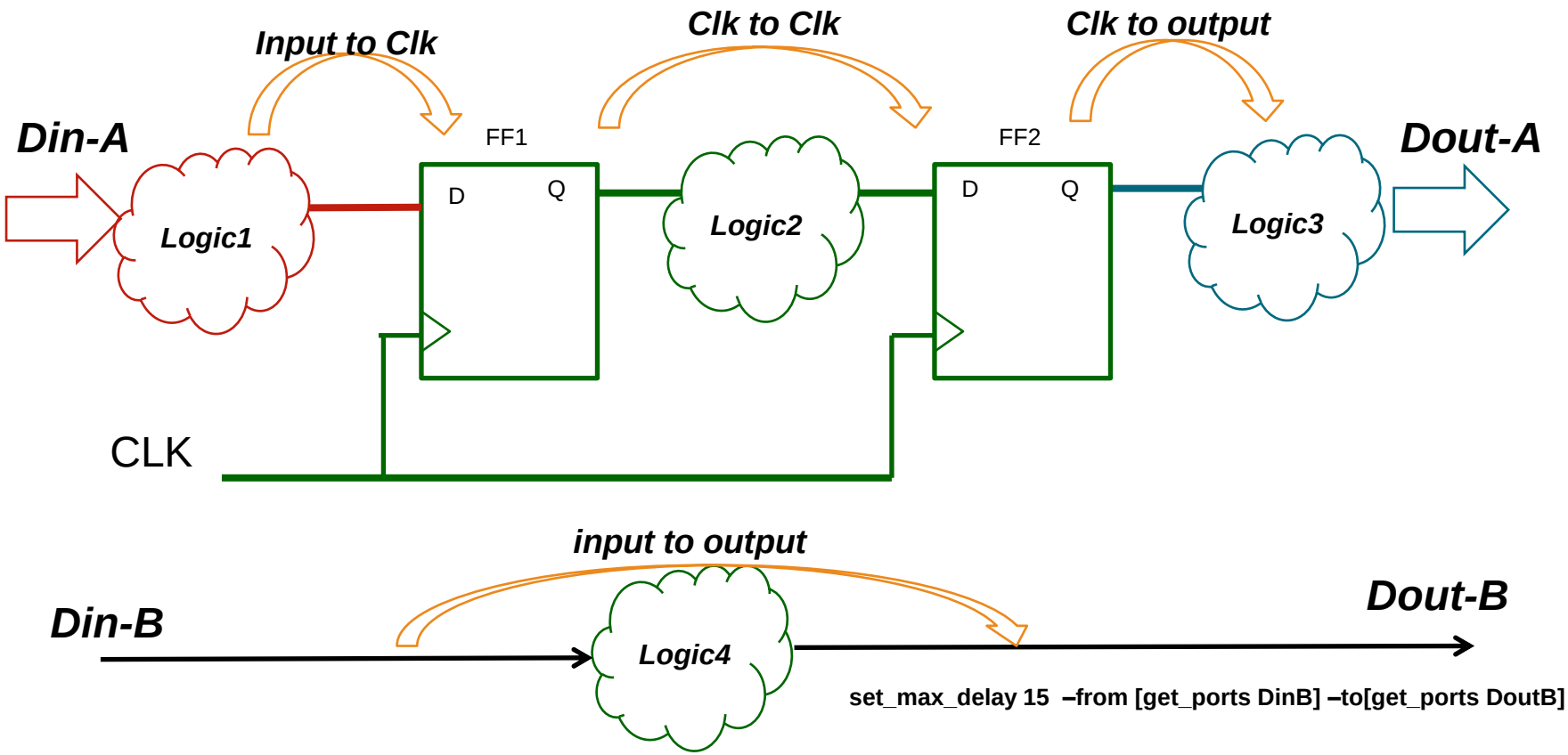
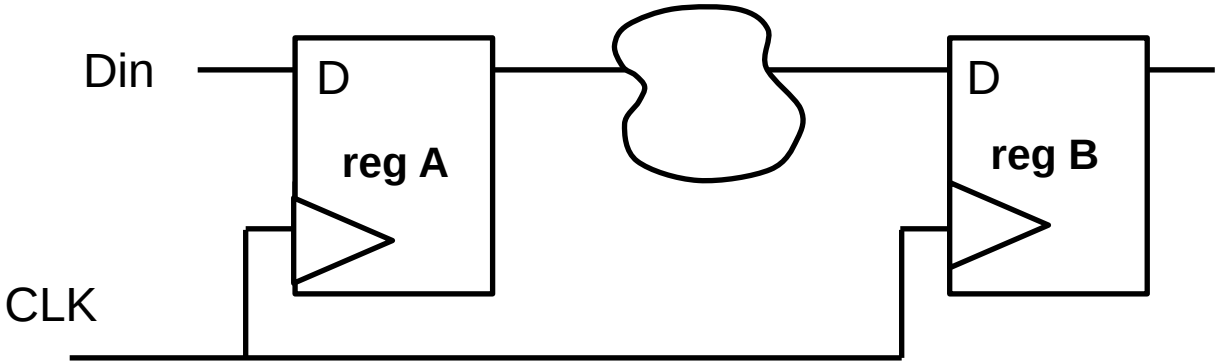
Timing Paths

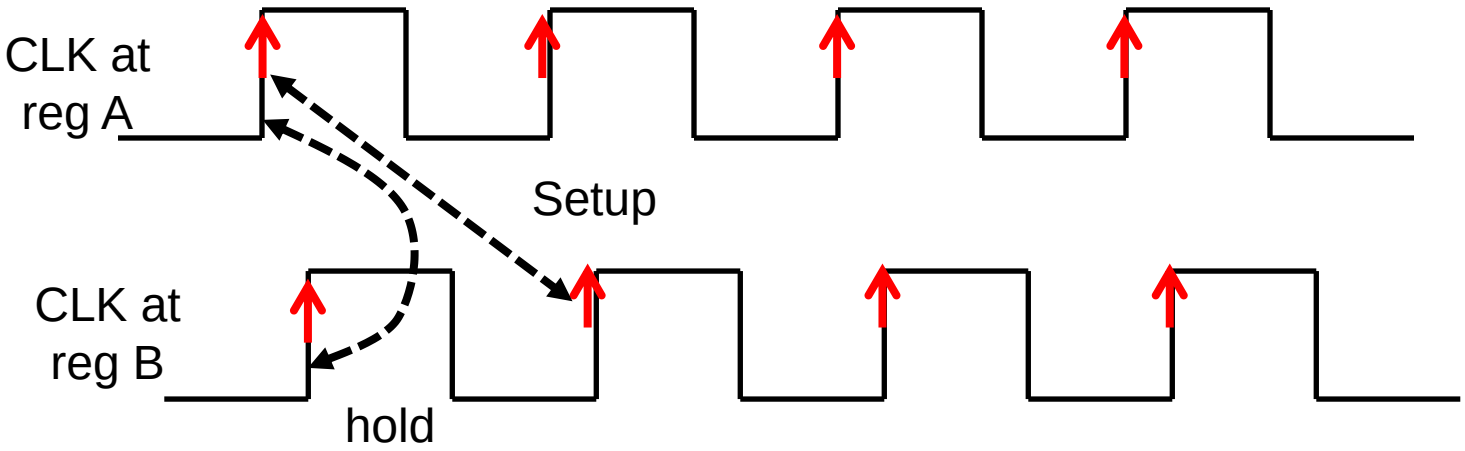
- These basic timing paths can apply to:
  - A module within an ASIC/FPGA
  - A whole ASIC/FPGA
  - A system with multiple chips



Timing Analysis: Setup/Hold Check

- **Create Clock: reg-to-reg requirement**

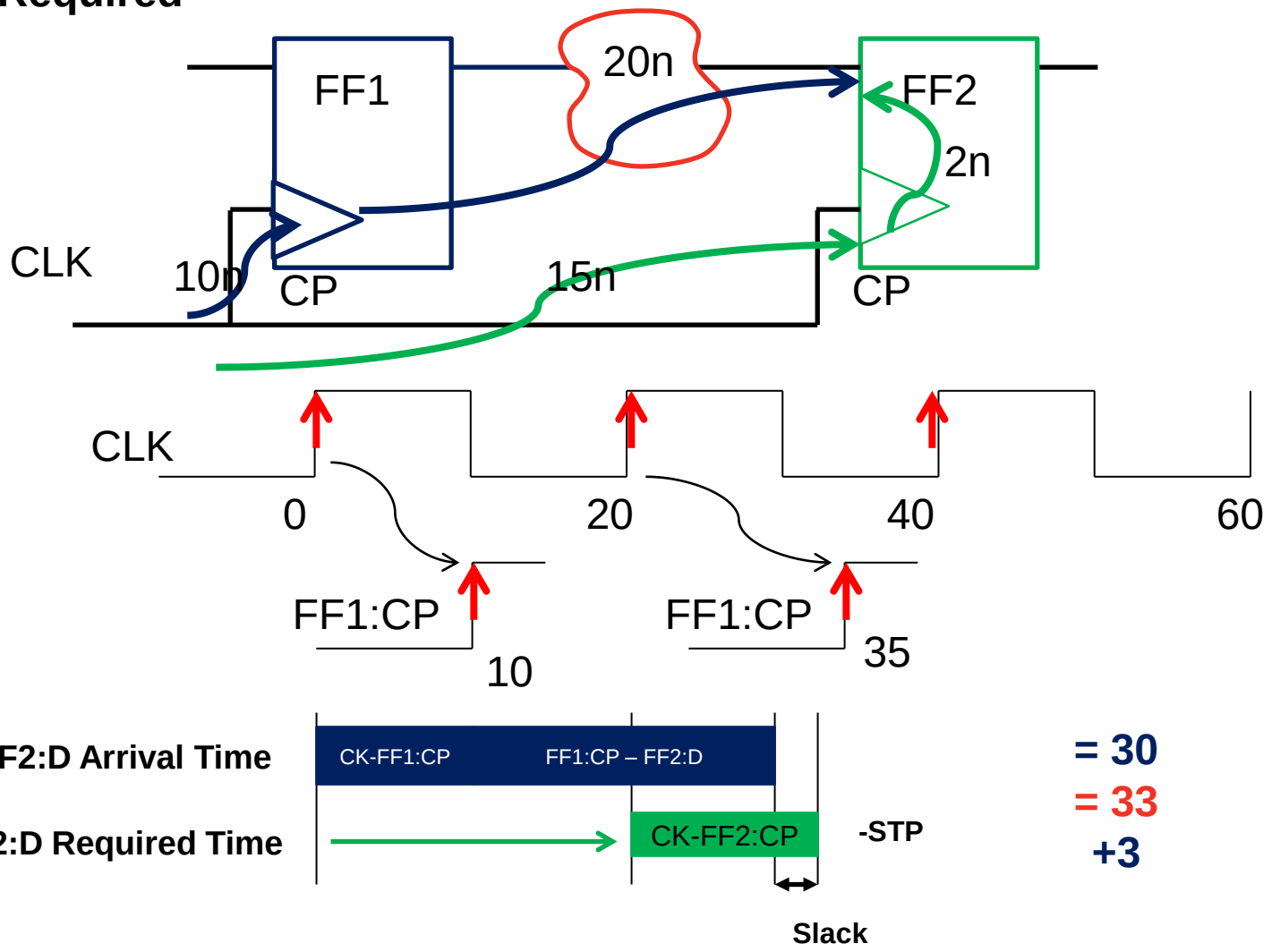




Single-cycle timing relationship

Setup Check

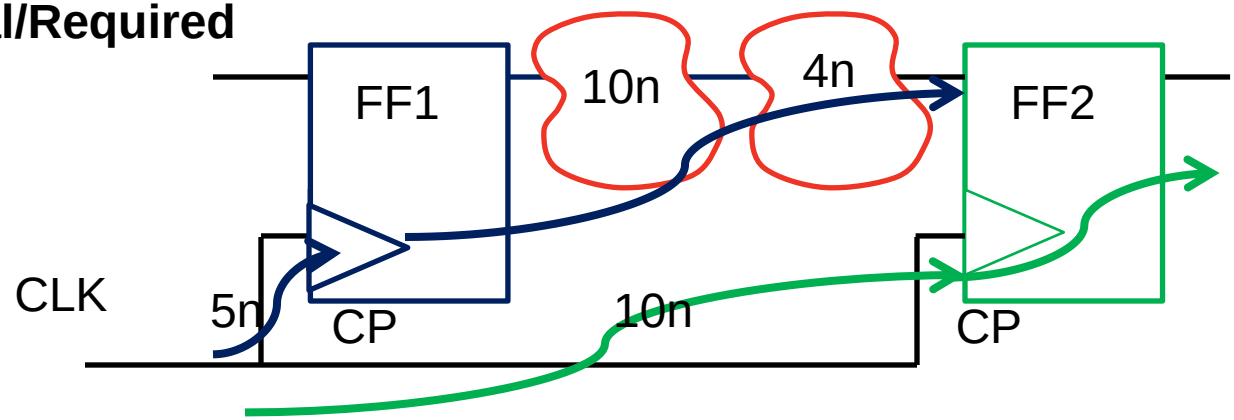
Arrival/Required

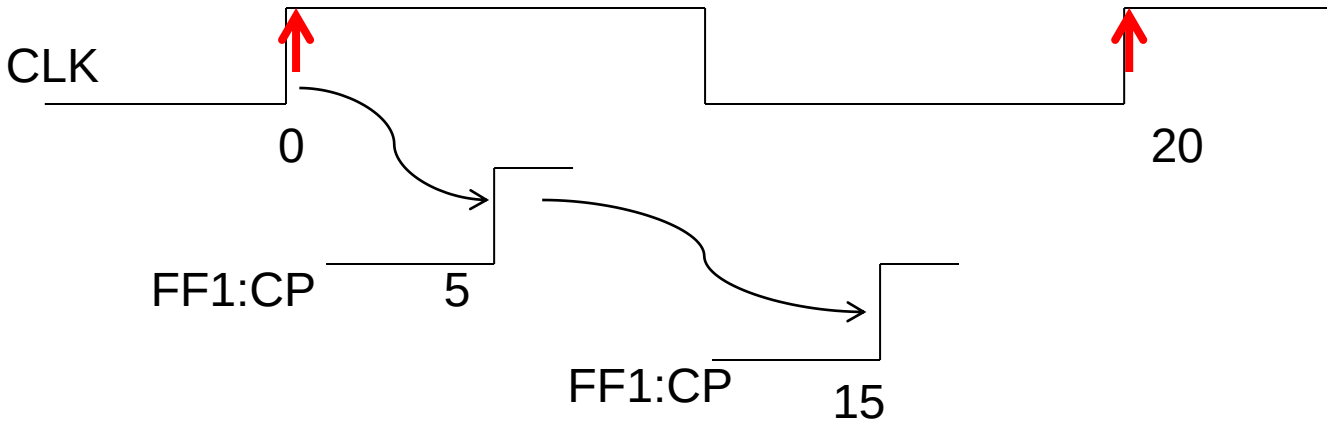


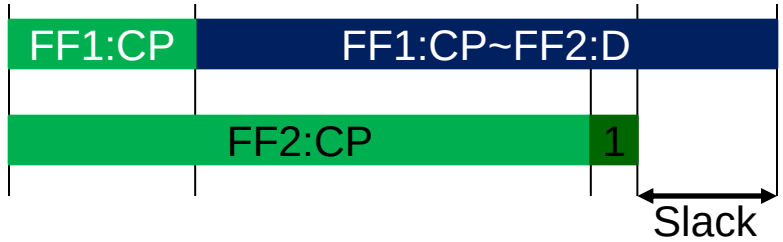
Slack = Required_time – Arrival_time (Violation if < 0)

Hold Check

Arrival/Required







= 19

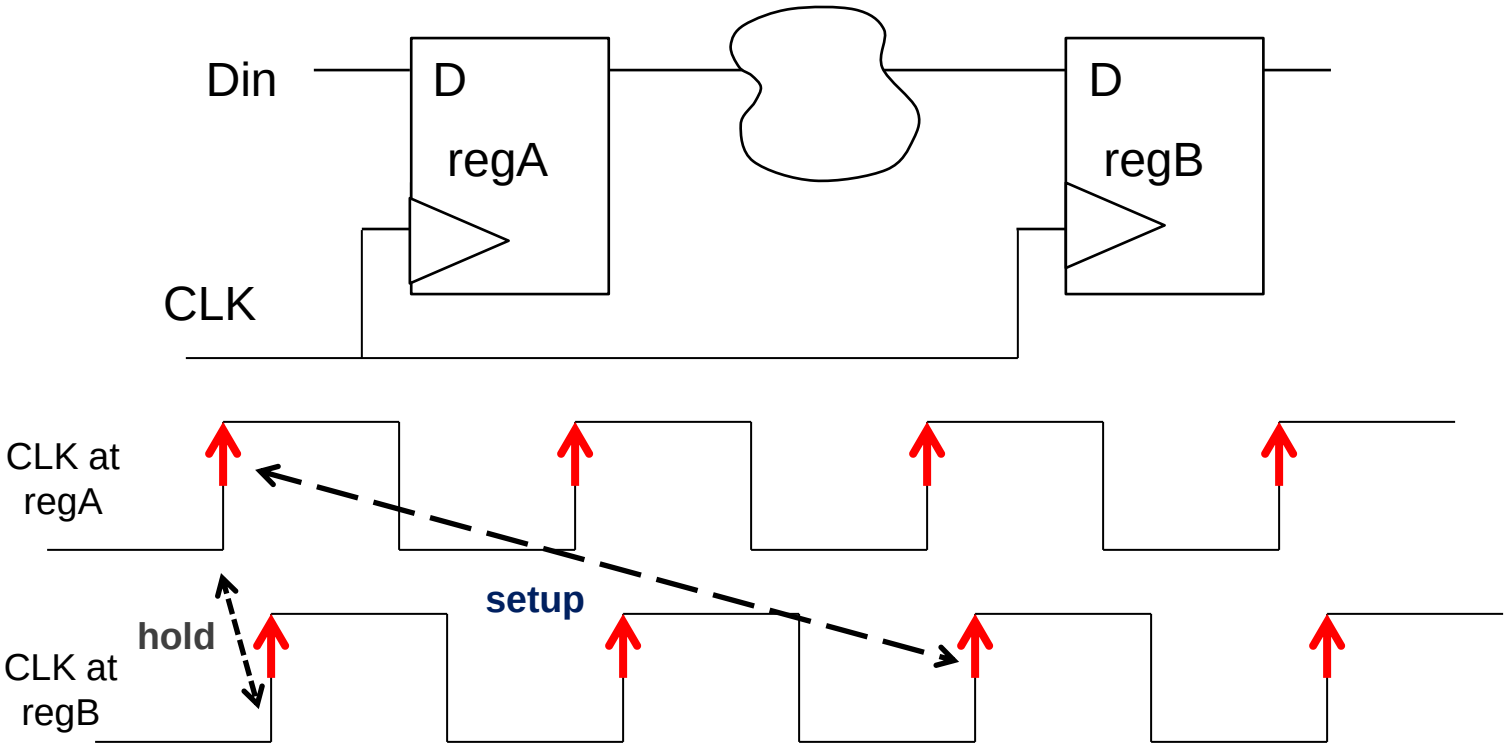
= 16

+3

Slack = ArrivalTime – RequiredTime (Violation if < 0)

Timing Analysis: Multi-cycle

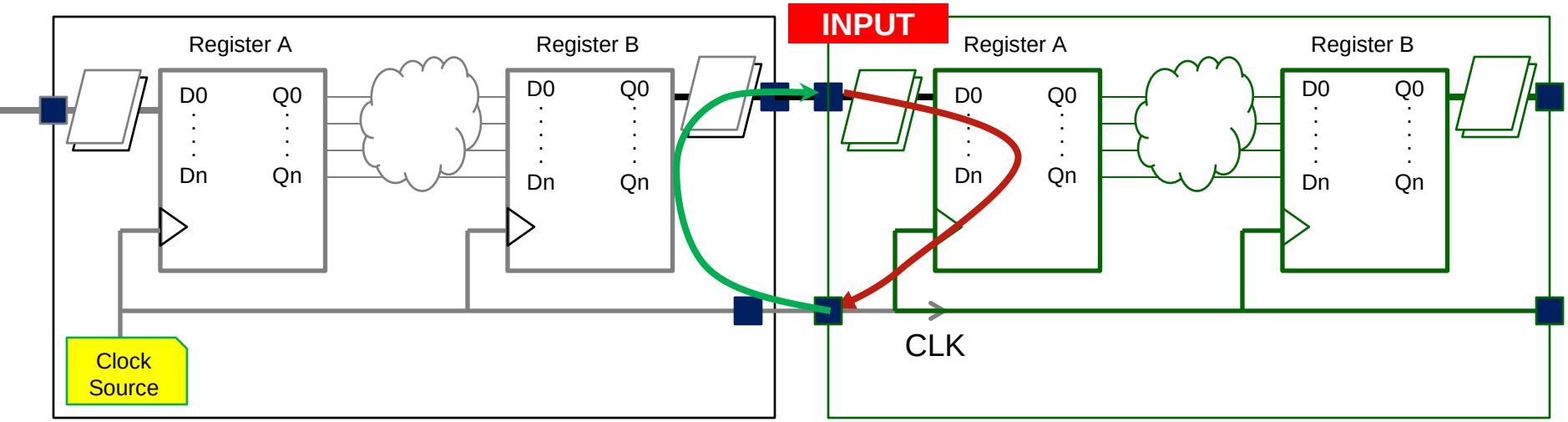
- set_multicycle_path -from [get_cells {1_reg[*]}] -to [get_cells {2_reg[*]}] 2
- set_multicycle_path -from [get_cells {1_reg[*]}] -to [get_cells {2_reg[*]}] -hold 1

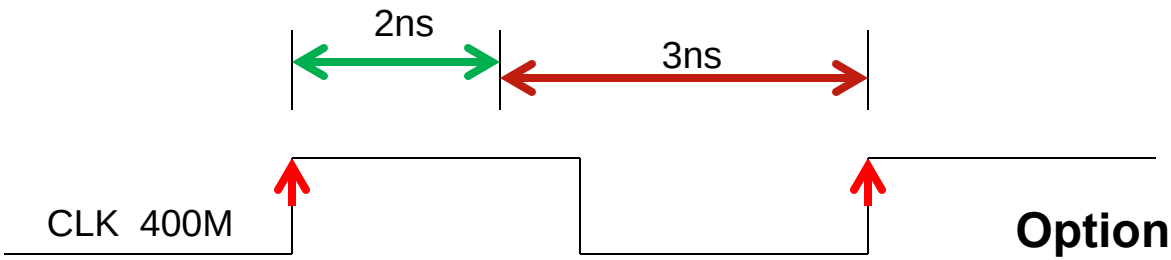


Multi-cycle timing relationship

Input Delay Constraints

- Captures External Setup/Hold Requirements



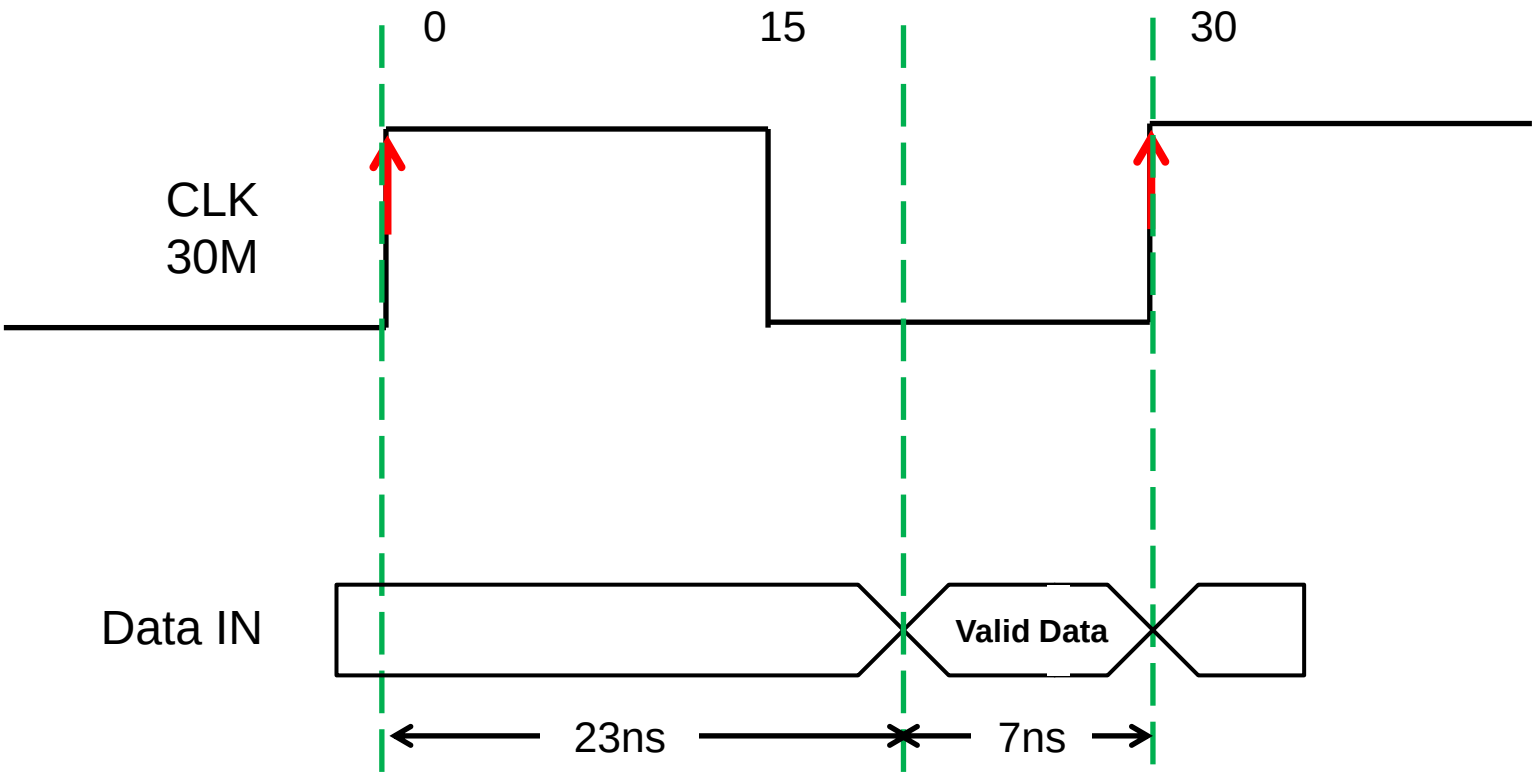


Option “-min” for hold check
Option “-max” for setup check

XDC: set_input_delay 2.0 -clock CK {IN}

Constraining Designs

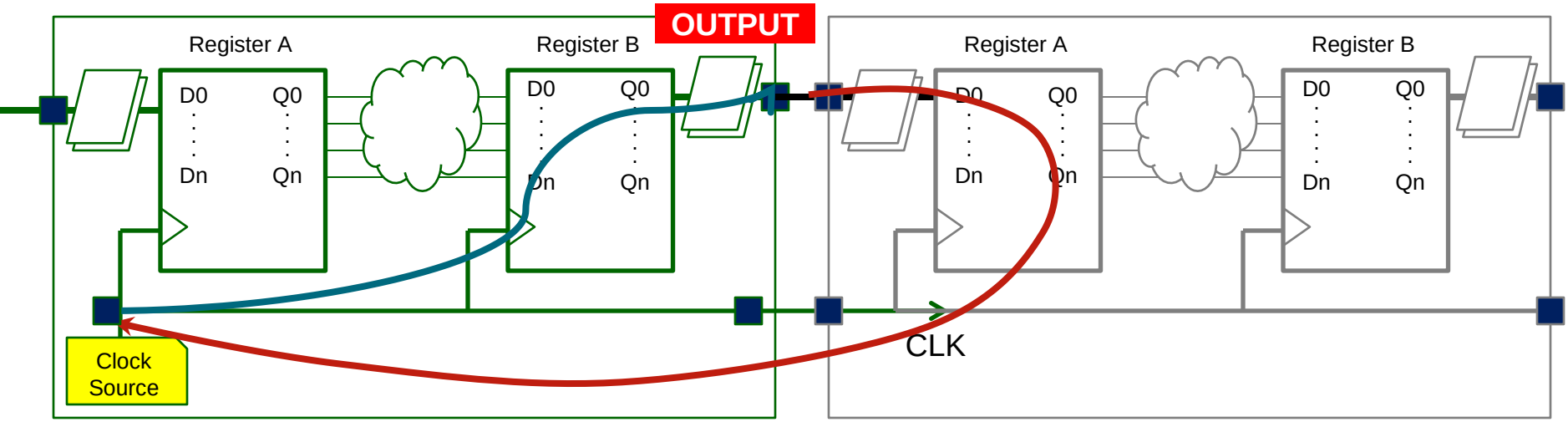
- **Set Input Delay: setup/hold requirements**

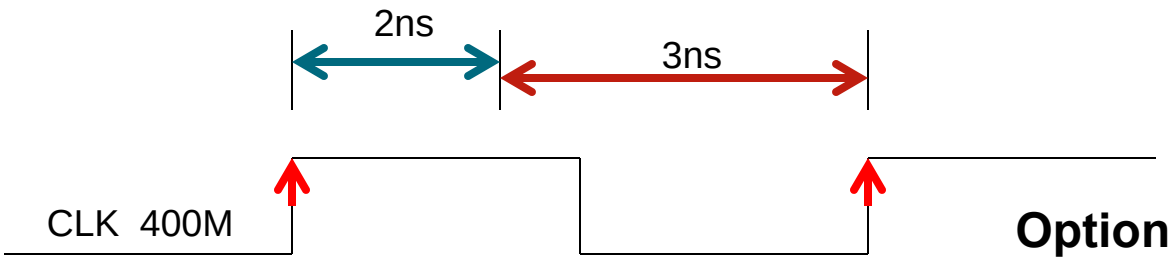



```
set_input_delay -max 23.0 -min 0.0 -clock clk {datain}
```

Output Delay Constraint

- Captures Clock-to-Out Requirements



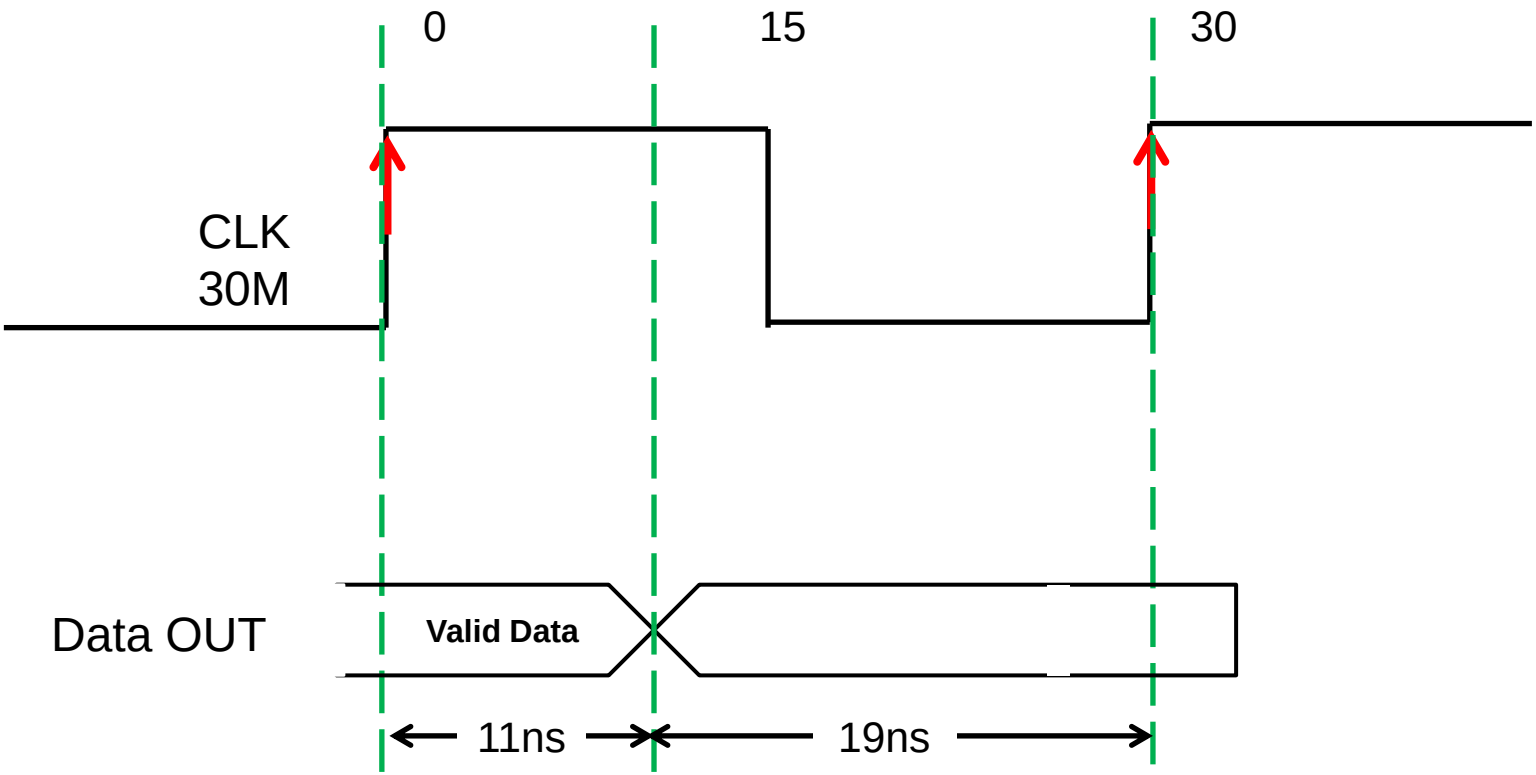


Option “-min” for hold check
Option “-max” for setup check

XDC: set_output_delay 3.0 -clock CK {OUT}

Constraining Designs

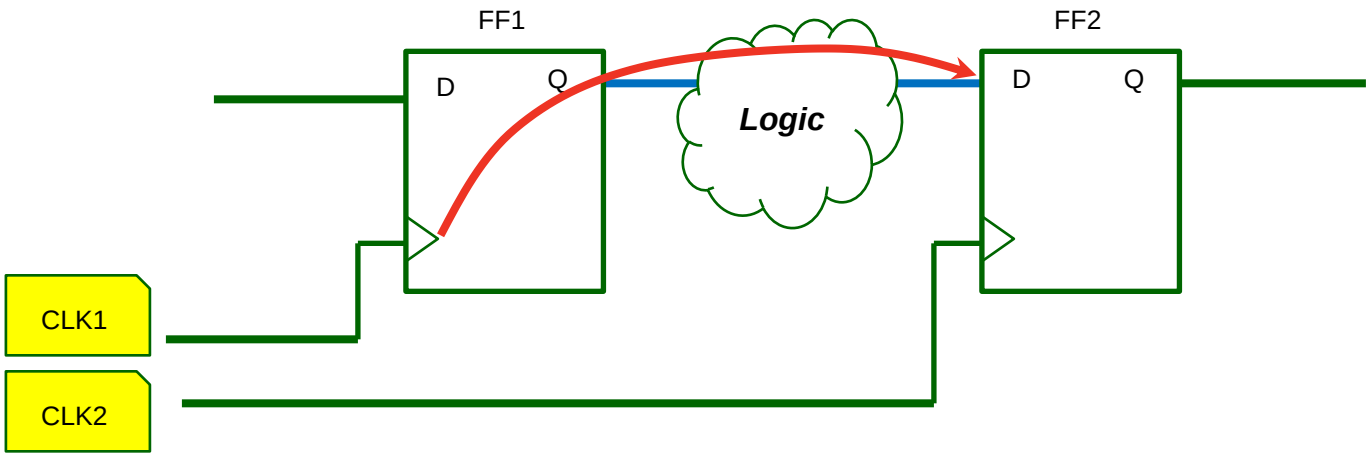
- **Set output Delay: Clock-to-out requirements**



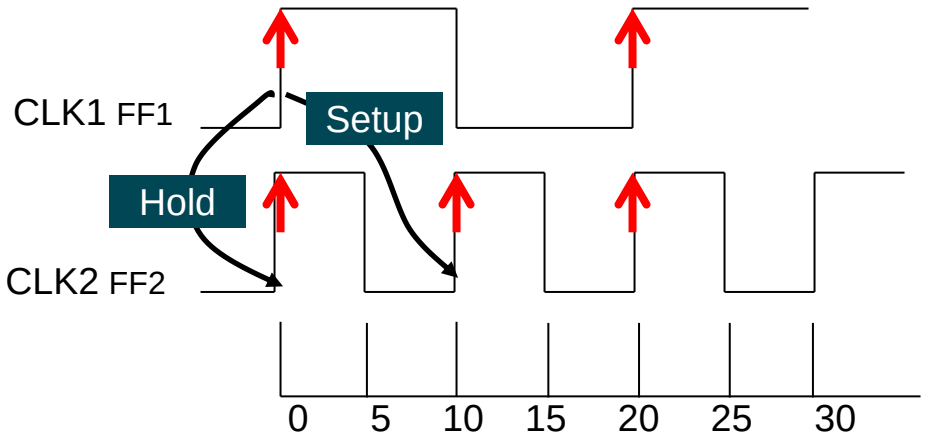
set_output_delay -max 19.0 -clock clk {dataout}

Cross-Domain Analysis

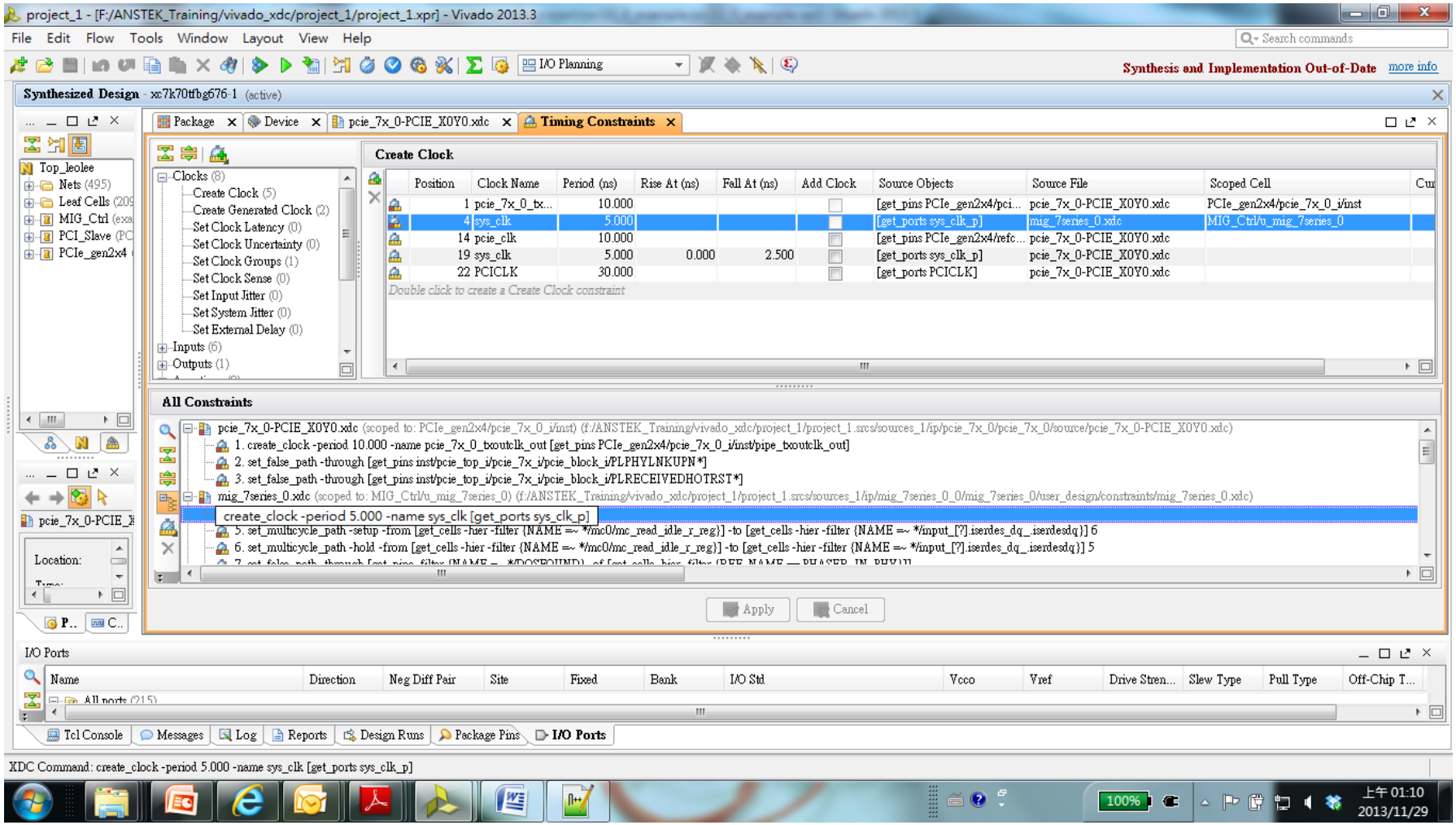
- **Study over the Least Common Multiplier**



XDC : creat_clock –period 20 –waveform { 0 10} CLK1
XDC : creat_clock –period 10 –waveform { 0 5 } CLK2

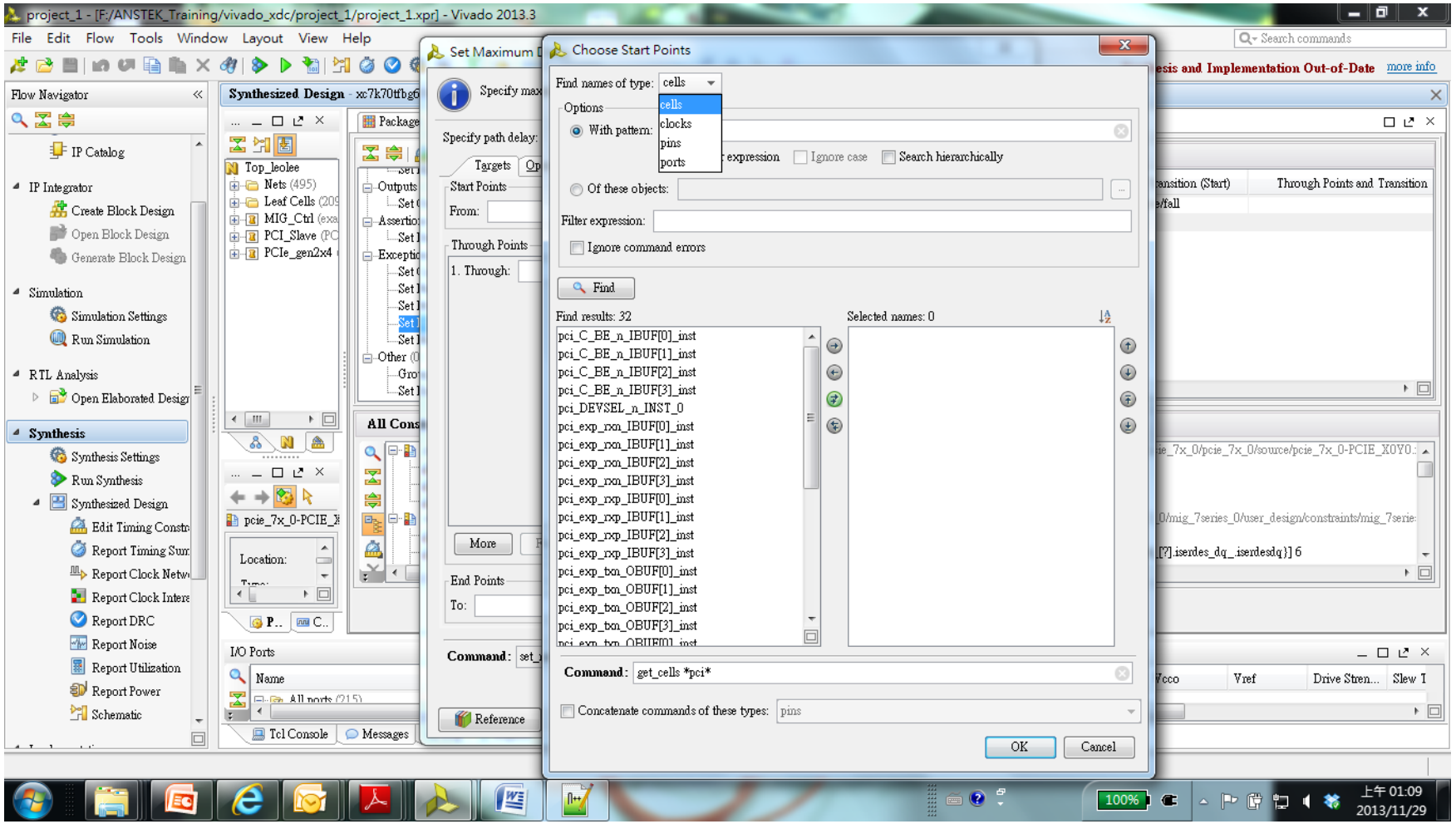


Vivado Timing Edit



Vivado GUI Interface

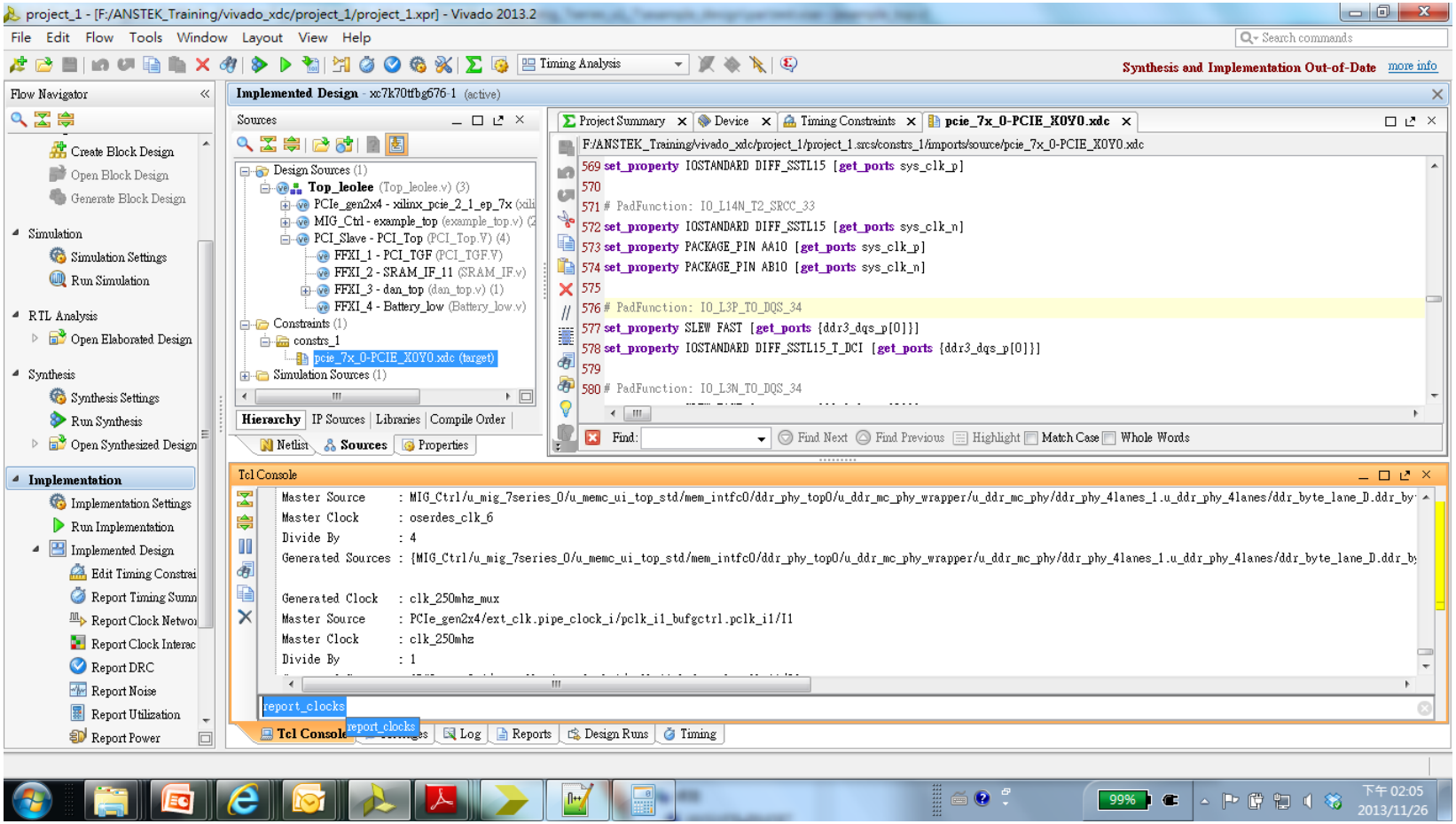
Cells/Clock/Pins/Ports

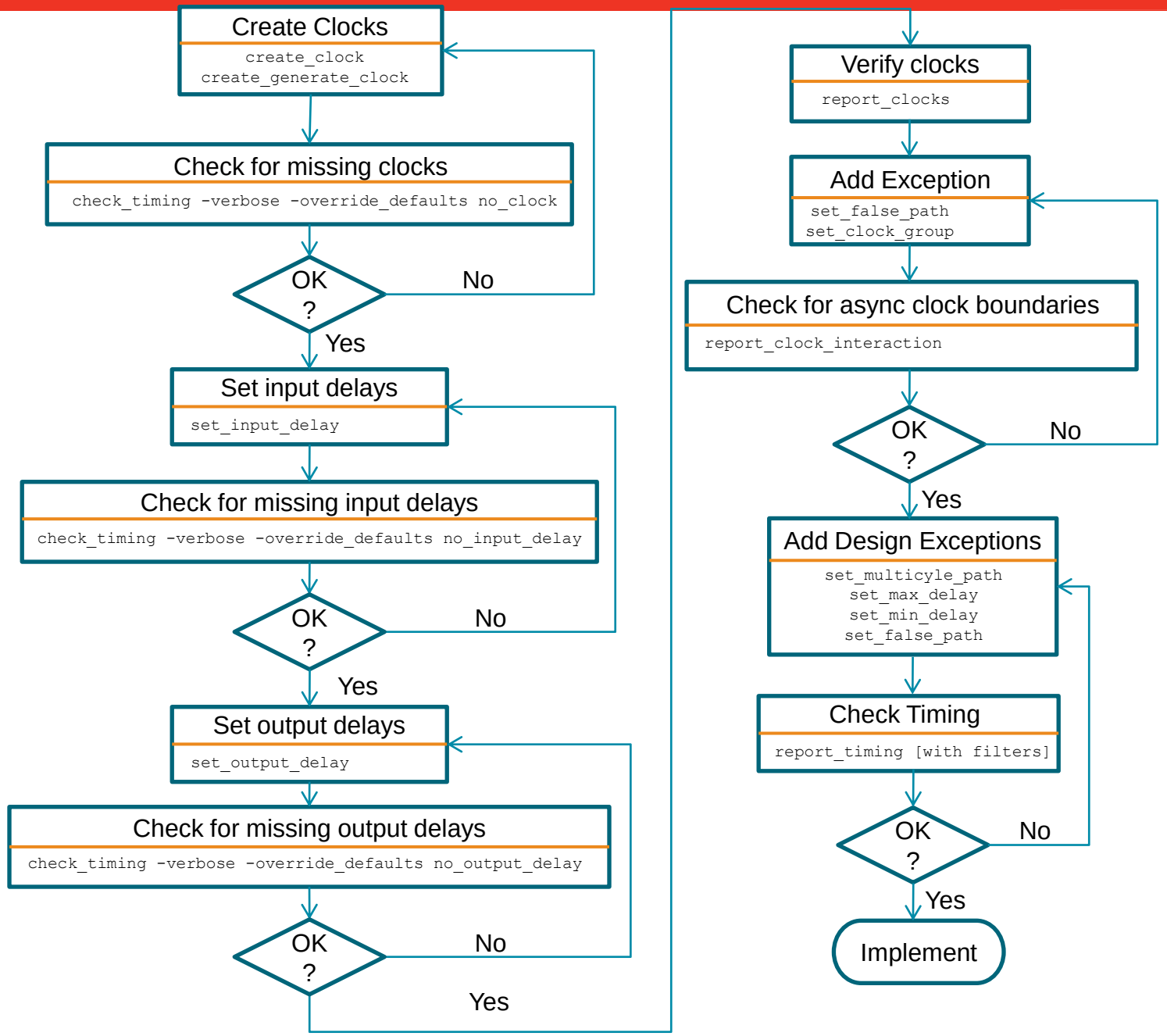


TCL Command Windows

% help –category <name>

- gives list and brief description of commands in that category





More Info

- *ISE to Vivado Design Suite Migration Guide*
- *Migrating UCF* Constraints to XDC – YouTube
- *Vivado Design Suite Tcl Command Reference Guide*
- *Vivado Design Suite User Guide / Using Constraints*
- *Vivado Design Suite Properties Reference Guide*
- *Vivado Design Suite User Guide Programming and Debugging*