Xilinx ZYNQ PCB point list

『 ———————————— **Power 部份** ———————————— 』

ZYNQ 是有 power sequence 的要求,原則上只要比照 7 series 就可以了.

Table 2-1: **Power Pins**

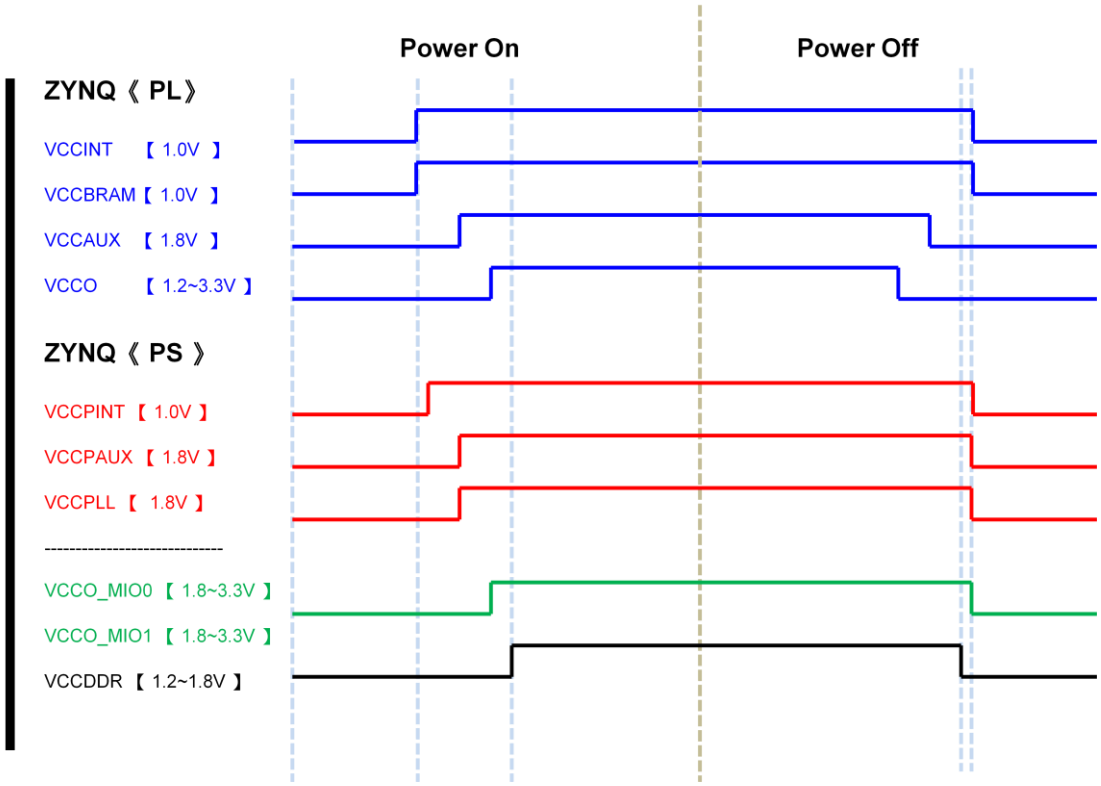
Type	Pin Name	Nominal Voltage	Power Pin Description
PS Power	V_{CCPINT}	1.0V	Internal logic
	V_{CCPAUX}	1.8V	I/O buffer pre-driver
	V_{CCO_DDR}	1.2V to 1.8V	DDR memory interface
	V_{CCO_MIO0}	1.8V to 3.3V	MIO bank 0, pins 0:15
	V_{CCO_MIO1}	1.8V to 3.3V	MIO bank 1, pins 16:53
	V_{CCPLL}	1.8V	Three PLL clocks, analog
PL Power	V_{CCINT}	1.0V	Internal core logic
	V_{CCAUX}	1.8V	I/O buffer pre-driver
	$V_{CCO\_\#}$	1.8V to 3.3V	I/O buffers drivers (per bank)
	V_{CC_BATT}	1.5V	PL decryption key memory backup
	V_{CCBRAM}	1.0V	PL block RAM
	$V_{CCAUX\_IO\_G\#}$	1.8V to 2.0V	PL auxiliary I/O circuits
XADC	VCCADC, GNDADC	N/A	Analog power and ground.
Ground	GND	Ground	Digital and analog grounds

http://www.xilinx.com/support/documentation/data_sheets/ds187-XC7Z010-XC7Z020-Data-Sheet.pdf

http://www.xilinx.com/support/documentation/data_sheets/ds191-XC7Z030-XC7Z045-data-sheet.pdf

ZYNQ 的 DC Datasheet 有兩份,針對有無 Transceiver 的系列是不同的

Xilinx ZC702 Power Sequence



ZYNQ 有一些 IO 介面的 Hardcore IP 可以使用,這些 I/O 是可以藉由軟體來定義出 PIN 的位置(由 PS),因為 ZYNQ 在 PS I/O 介面有 MUX 所以也能夠經由設定由 PL 出 PIN

Technical Reference Manual

http://www.xilinx.com/support/documentation/user_guides/ug585-Zynq-7000-TRM.pdf

Table 2-3: **I/O Peripheral MIO-EMIO Interface Routing *(Cont'd)***

Peripheral	MIO Routing	EMIO Routing	Cross Reference
USB [0,1]	Host, device, and OTG	Not available	See Chapter 15, USB Host, Device, and OTG Controllers
Ethernet [0,1]	RGMII v2.0	MII/GMII(1)	See Chapter 16, Gigabit Ethernet Controller
SPI [0,1]	50 MHz	Available	See Chapter 17, SPI Controller
CAN [0,1]	ISO 11898 -1, CAN 2.0A/B	Available	See Chapter 18, CAN Controller
UART [0,1]	Simple UART: Two pins (TX/RX)	TX, RX, DTR, DCD, DSR, RI, RTS and CTS	See Chapter 19, UART Controller
I2C [0,1]	SCL, SDA {0, 1}	SCL, SDA {0, 1}	See Chapter 20, I2C Controller
PJTAG	TCK, TMS, TDI, TDO	TCK, TMS, TDI, TDO, 3-state for TDO	See Chapter 27, JTAG and DAP Subsystem
Trace Port IU	Up to 16-bit data	Up to 32-bit data	See Chapter 28, System Test and Debug

Notes:

1. When the Ethernet MII/GMII interface is routed through EMIO, other MII interfaces (e.g., RMII, RGMII, and SGMII) can be derived using appropriate shim logic in the PL that attaches to PL pins.

ZYNQ's Packaging and Pinout

http://www.xilinx.com/support/documentation/user_guides/ug865-Zynq-7000-Pkg-Pinout.pdf

ZYNQ 外掛的 Flash 可以支持 Quad-SPI,如果需要更大的空間,也可以支持兩顆 Quad-SPI Flash

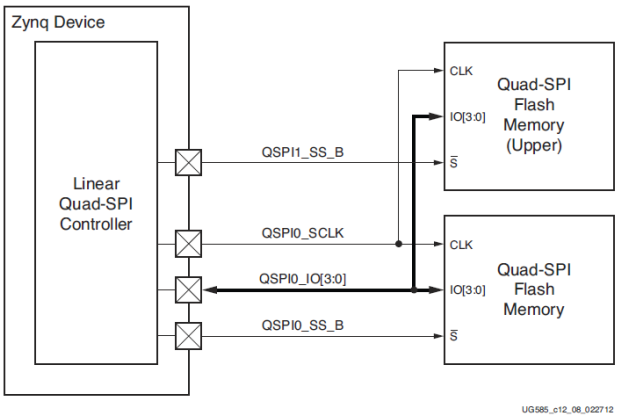


Figure 12-7: **Quad-SPI Dual SS 4-bit Stacked I/O**

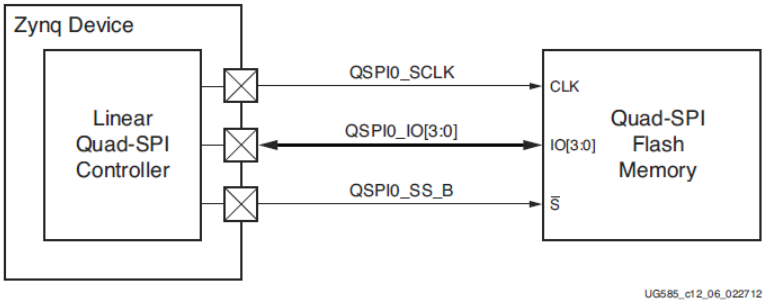


Figure 12-5: **Quad-SPI Single SS 4-bit I/O**

由於 ZYNQ 的 PL 是透過 PS 來 Config,所以相關的 Boot pin 都在 PS,而這些 PIN 都是 multi-function PIN,因此在初始化時需要有外部的硬體電路來作 Pull up/down 作設定（20K 的電阻是點）

6.2.5 Mode Pin Settings

Five mode pins, mode[4:0], are used to indicate the boot source, JTAG mode, and PLL bypass selection. Two voltage mode signals, VMODE[1:0], are used to indicate the voltage mode of the multiplexed I/O banks. The mode[4:0] and VMODE[1:0] signals should be connected using pull-up or pull-down 20 KΩ resistors. A pull-up resistor to V_{CCO_MIO0} specifies a 1 and a pull-down resistor to ground specifies a 0.

The VMODE signals are used to set the individual MIO_PIN registers to the appropriate LVCMOS18 or LVCMOS33 IO standard for all MIO pins while the ROM is running. After the boot ROM completes, the FSBL can change the I/O standard from LVCMOS to HSTL as needed. The VMODE[0] pin is used to set the I/O standard on Bank 0 and VMODE[1] is used to set the I/O standard on Bank 1.

Table 6-2: **Boot_Mode Strapping MIO Pins**

	VMODE[1]	VMODE[0]	BOOT_MODE [4]	BOOT_MODE [0]	BOOT_MODE [2]	BOOT_MODE [1]	BOOT_MODE [3]
	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]
Cascaded JTAG							0
Independent JTAG							1
Boot Devices							
JTAG				0	0	0	0
NOR				0	0	1	
NAND				0	1	0	
Reserved				0	1	1	
Quad-SPI				1	0	0	
Reserved				1	0	1	
SD Card				1	1	0	
Reserved				1	1	1	
PLL Mode							

- MIO[2] selects the JTAG mode
- MIO[5:3] selects the boot mode
- MIO[6] enables the PLLs
- MIO[8:7] configures the I/O bank voltage

Technical Reference Manual

http://www.xilinx.com/support/documentation/user_guides/ug585-Zynq-7000-TRM.pdf

Table 25-1: **CPU Clock Frequency Ratio Examples**

CPU Clock	6:2:1	4:2:1	Clock Domain Modules
CPU_6x4x	800 MHz (6 times faster than CPU_1x)	600 MHz (4 times faster than CPU_1x)	CPU clock frequency, SCU, and OCM arbitration
CPU_3x2x	400 MHz (3 times faster than CPU_1x)	300 MHz (2 times faster than CPU_1x)	L2 cache memory, APU timers
CPU_2x	266 MHz (2 times faster than CPU_1x)	300 MHz (2 times faster than CPU_1x)	I/O peripherals, central interconnect, master interconnect, slave interconnect, and OCM RAM
CPU_1x	133 MHz	150 MHz	I/O peripherals AHB and APB interface busses

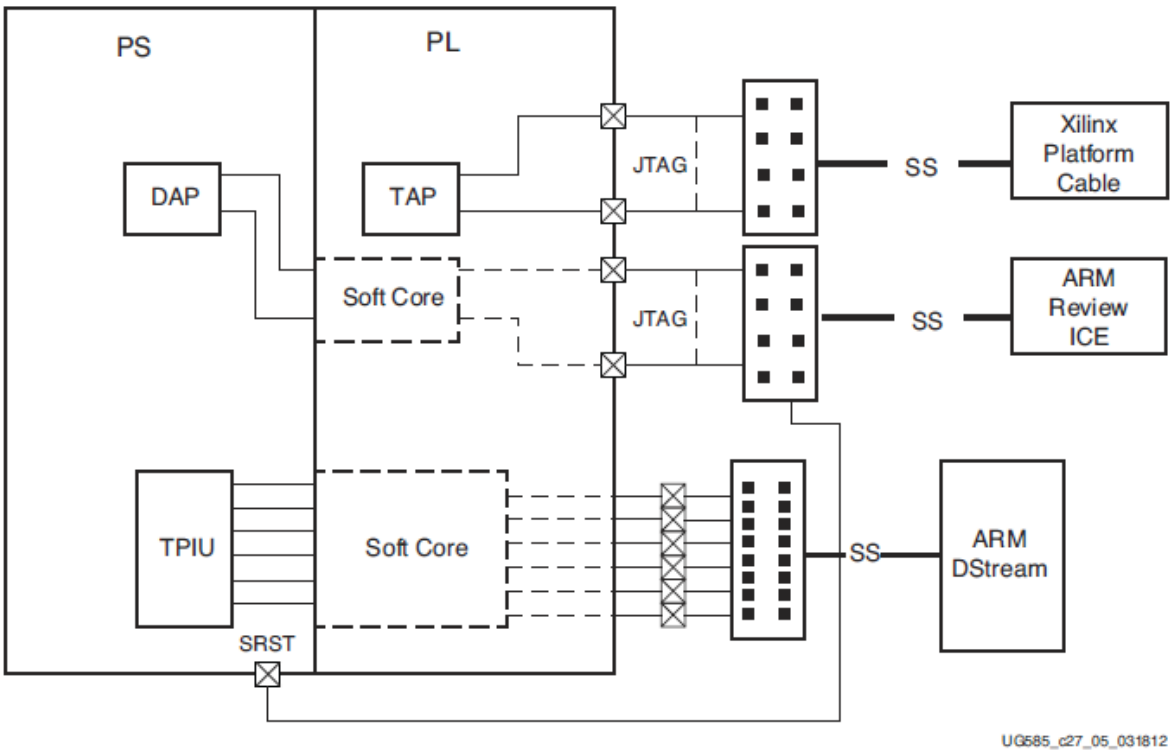
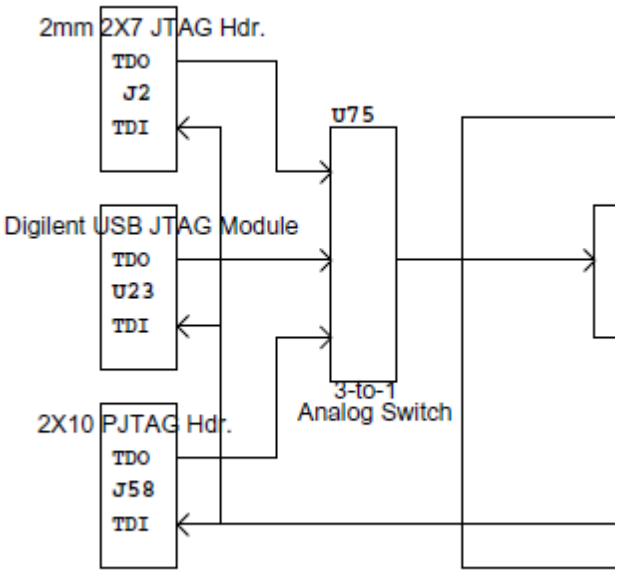


Figure 27-5: **User Case II: PS and PL Debug with Trace Port Enabled**



ZYNQ JTAG Chain 在公板上有三個不同的 cable 介面,是針對不 download cable,分別為 Xilinx/ARM/Digilent,但是真實的 **JTAG I/O 在 PL** 上只有一組

Table 2-2: **PS Signal Pins**

Group	Name	Type	Zynq-7000 Family Pin Count	7z010 CLG225 Pin Count	Voltage Node	Description
Clock	PS_CLK	I	1	1	V_{CCO_MIO0}	System reference clock. See Chapter 25, Clocks.
Reset	PS_POR_B	I	1	1	V_{CCO_MIO0}	Power on reset, active low. See Chapter 26, Reset System.
	PS_SRST_B	I	1	1	V_{CCO_MIO1}	Debug system reset, active Low. Forces the system to enter a reset sequence. See Chapter 26, Reset System.

PS_POR_B << 這 PIN 的功能是重新 download PS ARM 及 PL 的所有 Configuration ..
PS_SRST_B << 重新 Reset PS ARM 的 application,但是 Status 和 DDR 等的內容都會被保留...
這些 PIN 是可以參照公板線路先預留

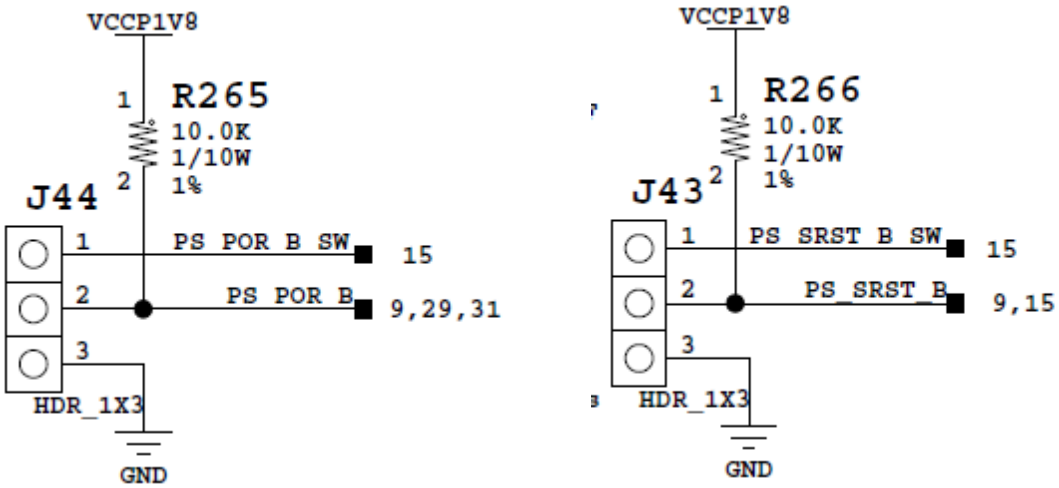


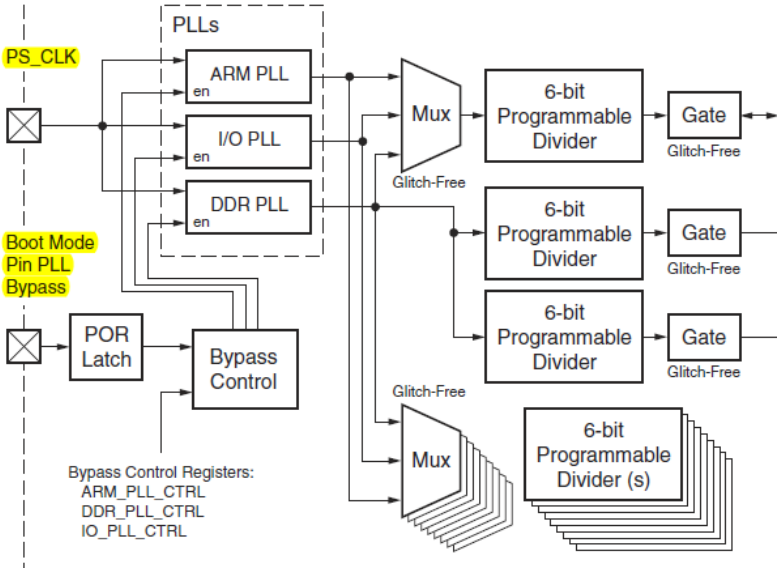
Table 6-2: **Boot_Mode Strapping MIO Pins *(Cont'd)***

	VMODE[1]	VMODE[0]	BOOT_MODE [4]	BOOT_MODE [0]	BOOT_MODE [2]	BOOT_MODE [1]	BOOT_MODE [3]
	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]
PLL Used			0				
PLL Bypassed			1				
MIO Bank 0 Voltage							
2.5 V, 3.3 V		0					
1.8 V		1					
MIO Bank 1 Voltage							
2.5 V, 3.3 V	0						
1.8 V	1						

MIO[6]主要的功能是選擇要不要開啟內部的 PLL,目前還沒看過有設定為 by pass...畢竟我們 33Mhz 輸入時需要再產生 3 組頻率..這三組要從別的地方再產生.似乎是更大的工程...

PCB Design and Pin Planning Guide << Xilinx 有提供一份 ZYNQ 專用的 PCB layiut guide
http://www.xilinx.com/support/documentation/user_guides/ug933-Zynq-7000-PCB.pdf

Technical Reference Manual
Figure 25-1.



ZYNQ 若沒有用到 ADC function 則以下 ADC pin 要如何處理?

DXN, DXP, VREFP, VREFN, VP, VN, VCCADC, GNDADC

VCCADC, GNDADC 兩 PIN 要接,VREFP, VREFN, VP, VN 可以選擇接地,VP, VN,至於這兩 PIN 其實是還好,沒特別規定

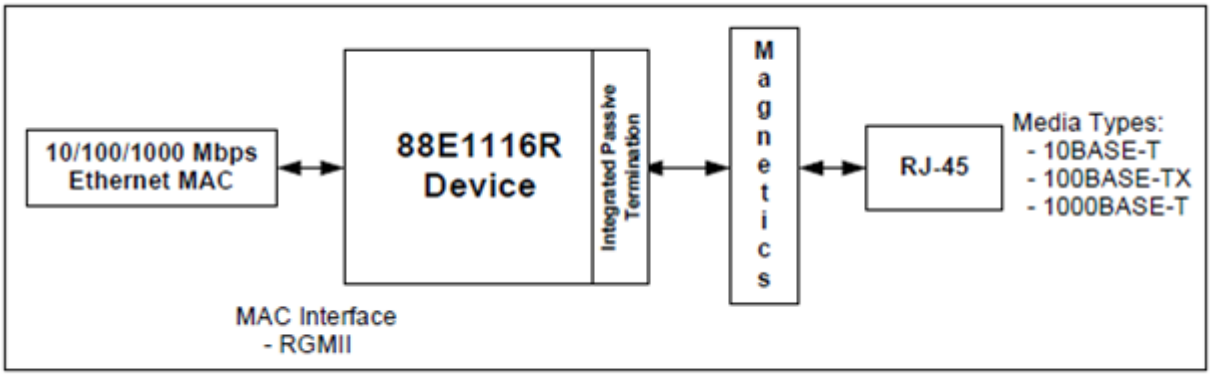
http://www.xilinx.com/support/documentation/user_guides/ug480_7Series_XADC.pdf

Table 1-1: **XADC Package PIns**

Package Pin	Type	Description
V_{CCADC_0}	Power supply	This is the analog supply pin for the ADCs and other analog circuits in the XADC. It can be tied to the 1.8V V_{CCAUX} supply however in a mixed-signal system the supply should be connected to a separate 1.8V analog if available. See Analog Power Supply and Ground (V_{CCADC} and GNDADC), page 69 for more information. This pin should never be tied to GND. The pin should be tied to V_{CCAUX} even if the XADC is not being used.
GNDADC_0	Power supply	This is the ground reference pin for the ADCs and other analog circuits in the XADC. It can be tied to the system ground via an isolating ferrite bead as shown in Figure 1-2. In a mixed-signal system this pin should be tied to an analog ground plane if available, in which case the ferrite bean is not required. See Analog Power Supply and Ground (V_{CCADC} and GNDADC), page 69 for more information. This pin should always be tied to GND even if the XADC is not being used.
V_{REFP_0}	Reference voltage input	This pin should be tied to an external 1.25V accurate reference IC (±0.2%) for best performance of the ADCs. It should be treated as an analog signal that together with the V_{REFN} signal provides a differential 1.25V voltage. By connecting this pin to GNDADC (see Figure 1-2) an on-chip reference source (±1%) is activated. This pin should always be connected to GNDADC if an external reference is not supplied. See Reference Inputs (V_{REFP} and V_{REFN}), page 69 for more information.
V_{REFN_0}	Reference voltage input	This pin should be tied to GND pin of an external 1.25V accurate reference IC (±0.2%) for best performance of the ADCs. It should be treated as an analog signal that together with the V_{REFP} signal provides a differential 1.25V voltage. This pin should always be connected to GND even if an external reference is not supplied. See Reference Inputs (V_{REFP} and V_{REFN}), page 69 for more information.
V_{P_0}	Dedicated analog input	This is the positive input terminal of the dedicated differential analog input channel (V_P/V_N). The analog input channels are very flexible and support multiple analog input signal types. For more information see Analog Inputs, page 26. This pin should be connected to GND if not used.
V_{N_0}	Dedicated analog input	This is the negative input terminal of the dedicated differential analog input channel (V_P/V_N). The analog input channels are very flexible and support multiple analog input signal types. For more information see Analog Inputs, page 26. This pin should be connected to GND if not used.

Q & A

Marvell 88E1116RA0 --- ZC702 PS



88E1116R Device used in Copper Application

National DP83640 ------- ISM Networking FMC Card

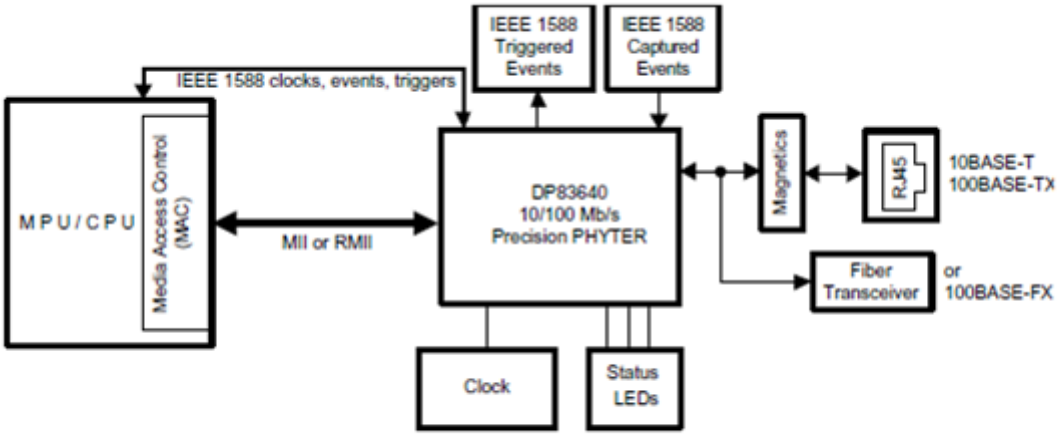


Figure 2-1. System Diagram

針對 AES 的功能,加密用的 Key 有兩種方法,如果用電池那斷電肯定不行的,這樣 Key 要重燒過(就是用 Xilinx 的燒錄軟體)
還有另一個用燒斷的方法.那也不用什麼電池了..反正就燒斷了,但這個 key 就不能再更改了..

32.2.9 AES Key Management

The AES encryption key is stored on-chip within the PL. It can be loaded into either volatile battery-backed RAM (BBRAM) or in non-volatile eFuse storage. The keys are loaded into the PL via the JTAG interface using the iMPACT software. (See UG470, *7 Series FPGAs Configuration User Guide* for more information)

ANSTek Xilinx FAE Leo>Lee