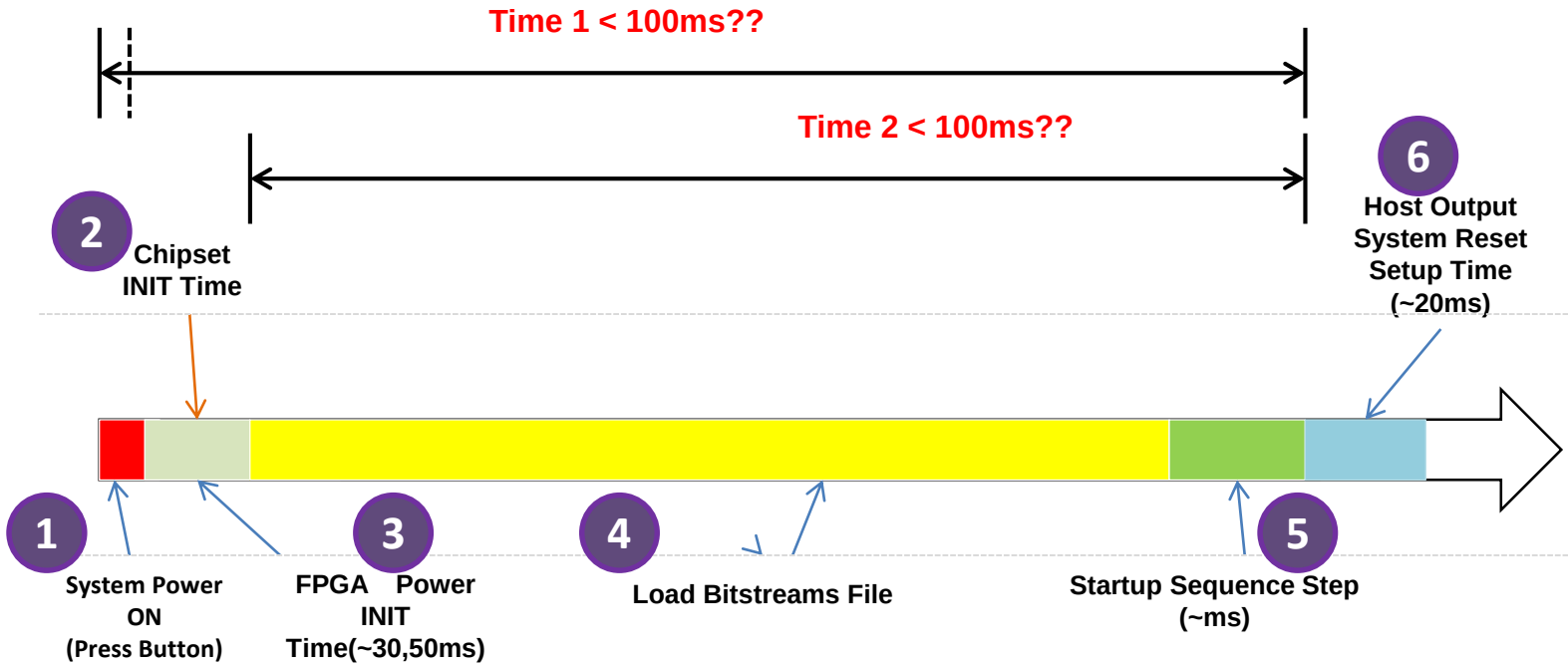
★漫談一直困擾著FPGA板卡界的PCIe認卡問題 – PCIe system reset time (100ms)



❶ 泛指系統的電源由按下啟動Power Supply開關點.

❷❸ 一般高階dvice都會有電源開關時序的問題,所以在這時間分別由大電開始轉小電所需時間,再則Chipset需要load Bios code時間,而FPGA需要初始化時間.

❹這一段時間就是FPGA load Bin file的時間,但這段時間確實是可以被FPGA的設置所改變的.

a.依照選擇的flash,如SPI/QSPO/BPI/Xilinx ROM,顯而易見,Date bit越多的裝置會越快.

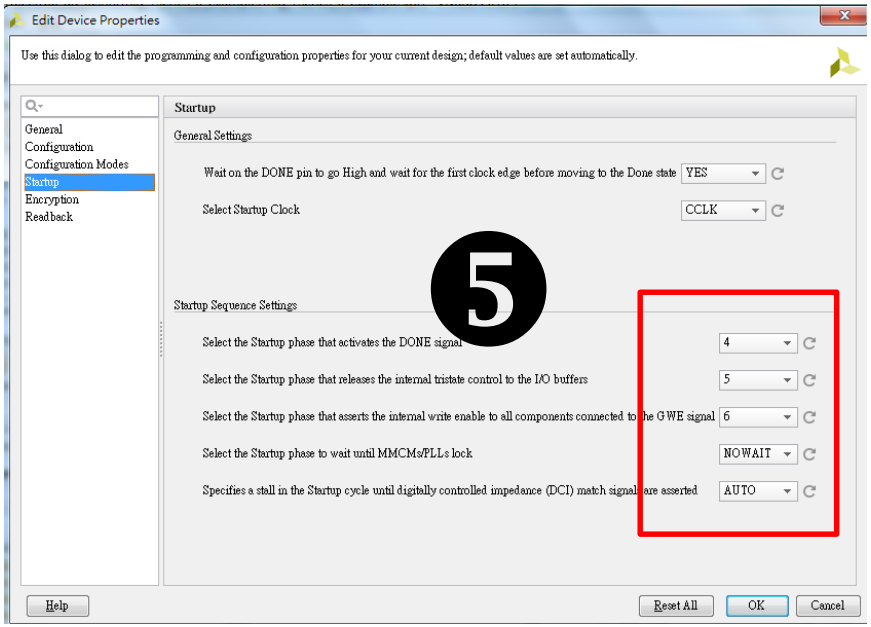
b.在constraint中設置FPGA輸出load code的CCLK速度,目前軟體能設的速度最快是66Mhz.

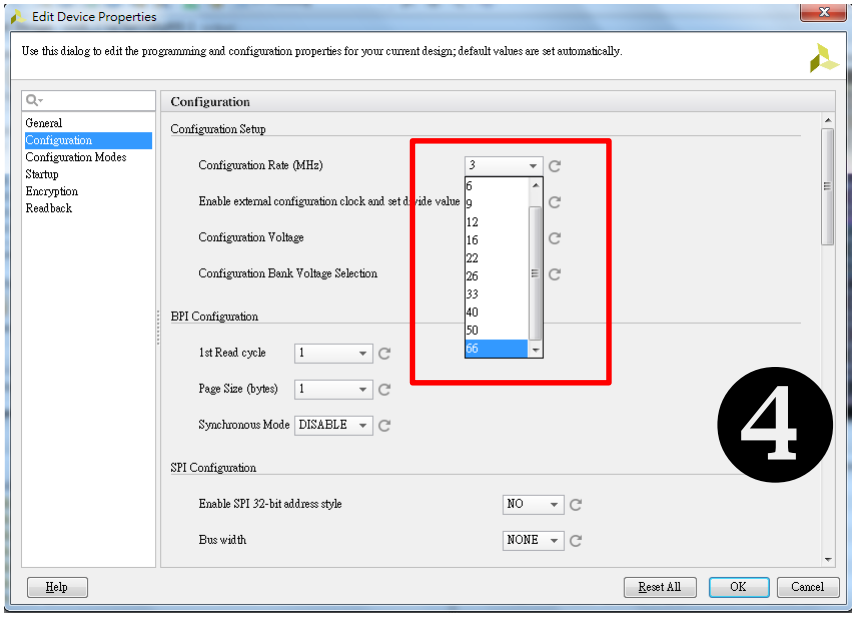
c.利用FPGA特定的IO PIN(EMCCLK)取代FPGA內部輸出的CCLK,這最快是120Mhz.

d.使用FPGA特有的【Partial Reconfiguration】或【Tadem feature】,先讓PCIe Core ready training,再第二階段的將user design載入FPGA.再則利用Xilinx 軟體設定壓縮,將Bin file變小也是一個方案(在此壓縮的定義並不是壓縮解壓縮的概念)

❺這一段時間是FPGA作完CRC check後,需要一段時間去作IO/PLL/BRAM等原件的初始化時間.這時間一般需要ms的時間,基於FPGA的Utilization會有不同的時間,另外值得一提的DONE PIN的完成並不全然表示FPGA已經能正常運作了.

❻ 在PCIe的規範中Chipset會在ready後的100ms開始scan system device,這段區間約為20ms





Configuration Switching Characteristics

Table 71: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade					Units
		1.0V			0.95V	0.9V	
		-3	-2/-2LE	-1/-1M	-2LI	-2LE	
Power-up Timing Characteristics							
T_{PL} (1)	Program latency	5	5	5	5	5	ms, Max
T_{POR} (1)	Power-on reset (50 ms ramp rate time)	10/50	10/50	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1 ms ramp rate time)	10/35	10/35	10/35	10/35	10/35	ms, Min/Max
$T_{PROGRAM}$	Program pulse width	250	250	250	250	250	ns, Min

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EMCCLK	14	Multi-function	Input	External Master Configuration Clock Optional external clock input for running the configuration logic in a master mode (versus the internal configuration oscillator). See Setting Configuration Options in the Vivado Tools, page 36 for more information. • For master modes: The FPGA can optionally switch to EMCCLK as the clock source, instead of the internal oscillator, for driving the internal configuration engine. The EMCCLK frequency can optionally be divided via a bitstream setting (ExtMasterCclk_en) and is forwarded for output as the master CCLK signal. • For JTAG and slave modes: EMCCLK is ignored in the JTAG and slave modes and can be left unconnected.

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『Bin load code時間估算』

xxx.bin size若為25Mbit
CCLK rate 設定為50Mhz

- ☐ SPI = ~500ms
- ☐ **QSPI = 25 ÷ 50 ÷ 4 = ~125ms**
- ☐ 2QSPI = 25 ÷ 50 ÷ 8 = ~62ms
- ☐ BPIx16 = ~31ms

Total configuration time:
EX: Tpor + load bin + startup sequence
30 + 125 + 10 = 160ms
※**Xilinx pcie tandem bin file size ~11Mbit**

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